Real time DSP

Professors:

- Eng. Julian S. Bruno
- Eng. Jerónimo F. Atencio
- Sr. Lucio Martinez

Analog to digital Converter

The BIG picture

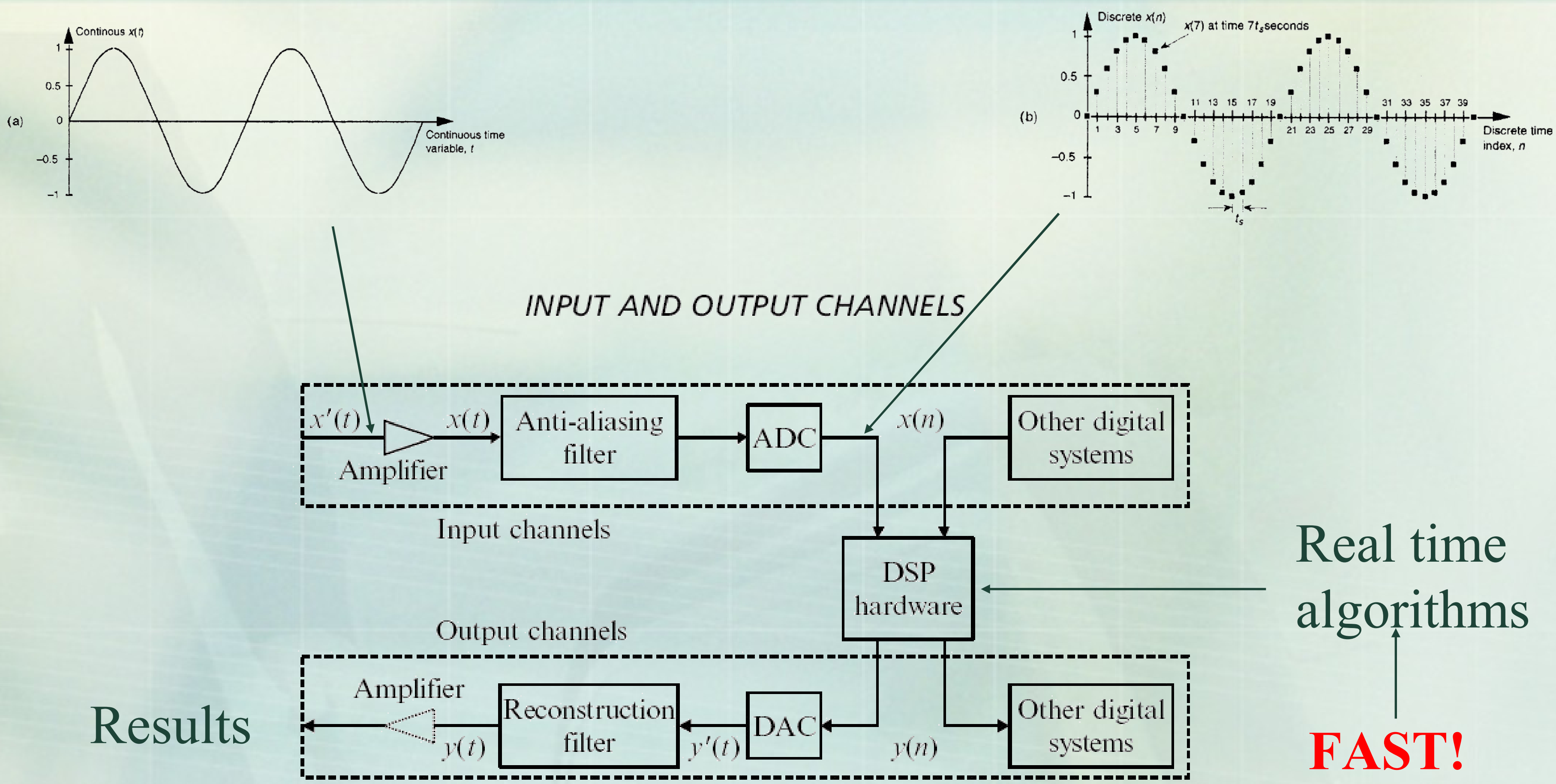
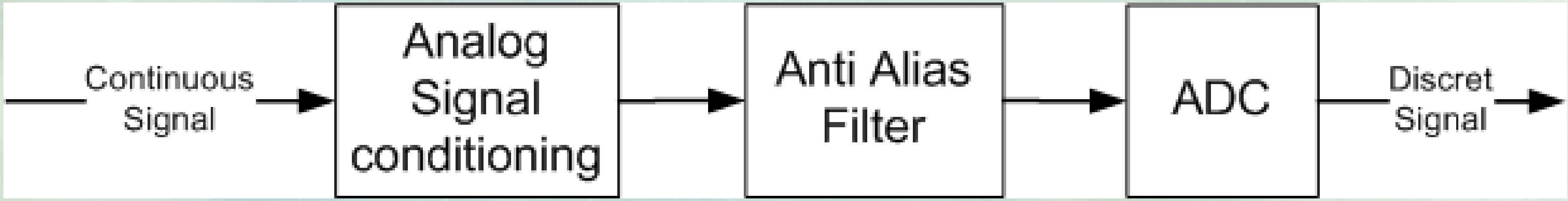


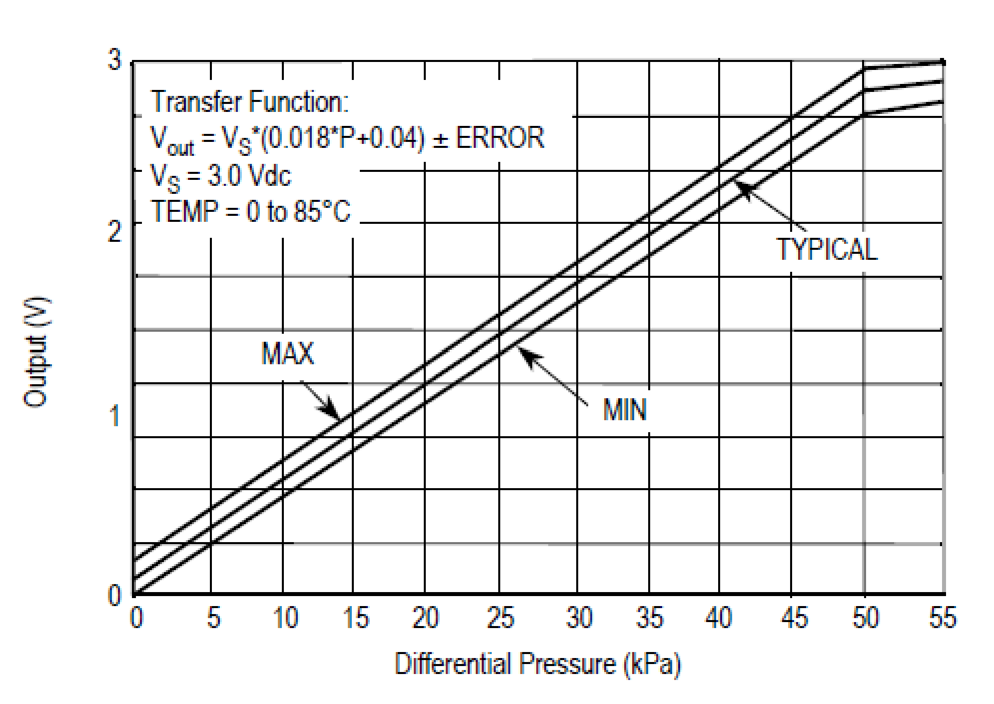
Figure 1.1 Basic functional blocks of real-time DSP system

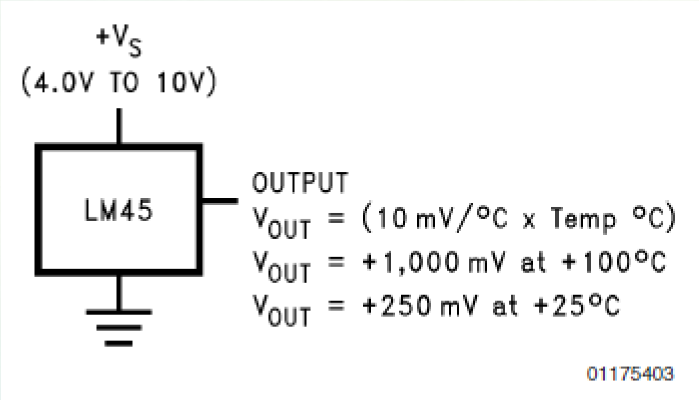
Signals

- Amplitude
- Frequency
- Noise

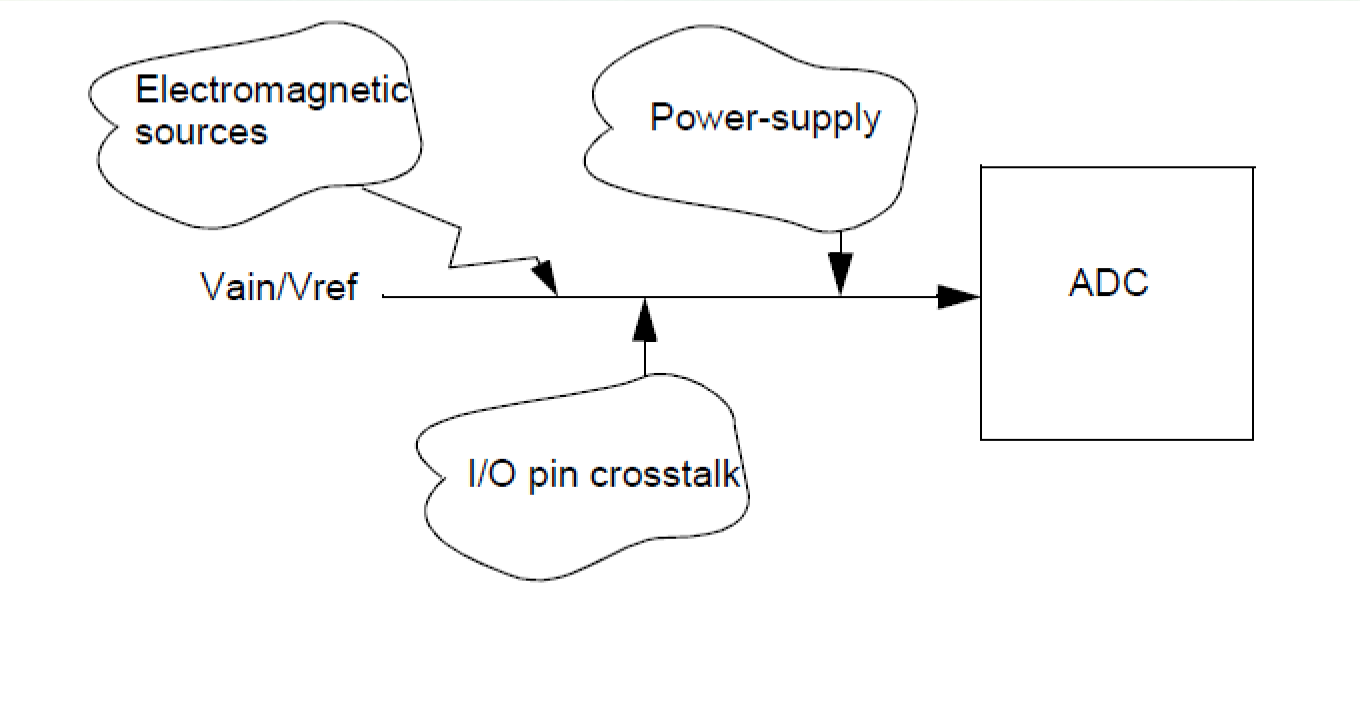


Continuous Signal

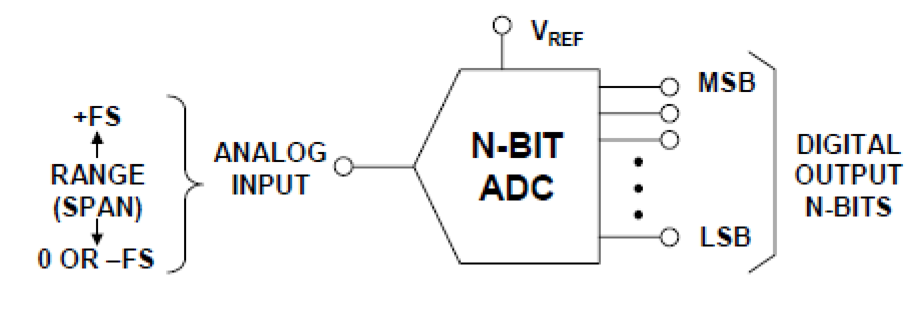




External Noise



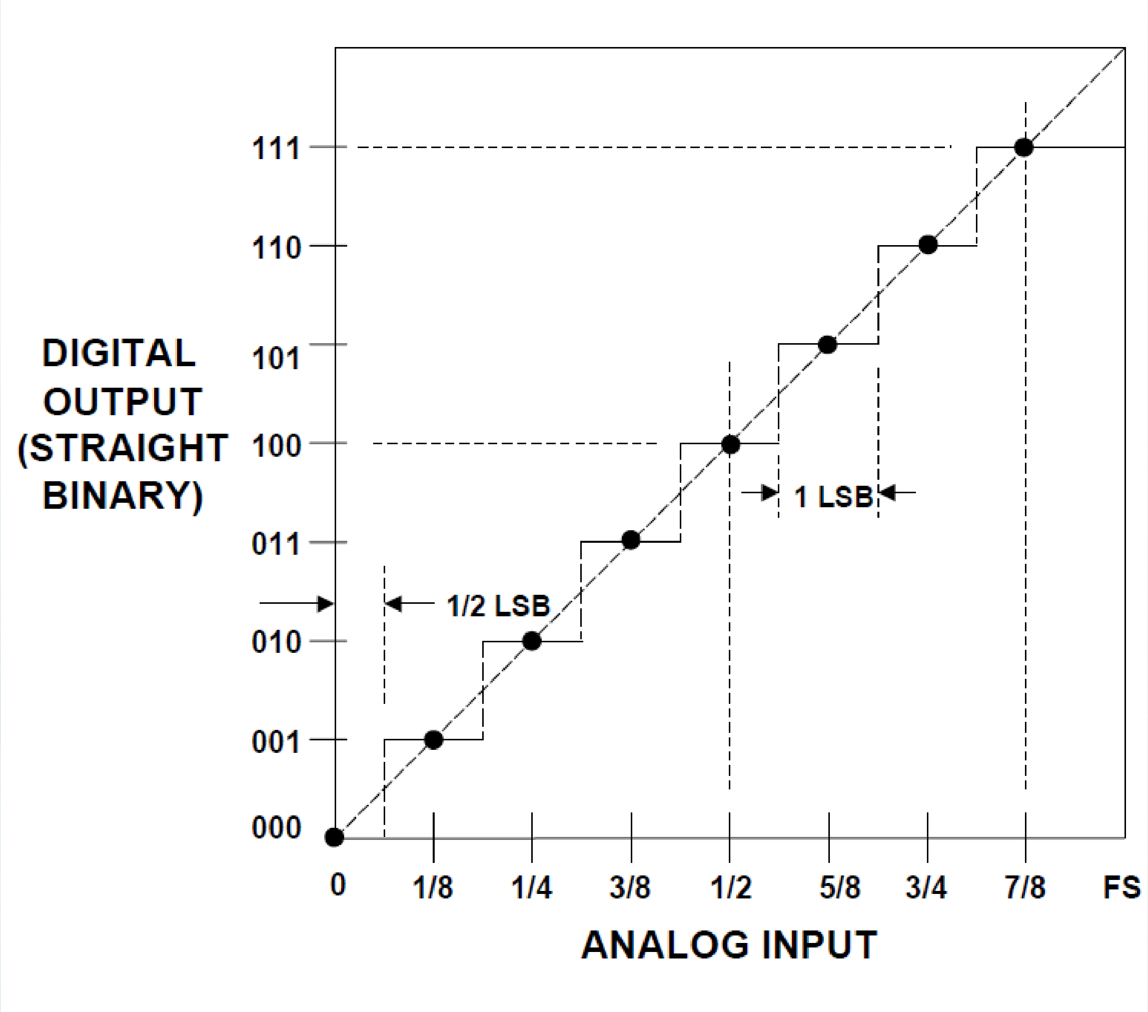
Quantization Noise



- Analog Input range: Vin = 0 to FS (Full Scale)
- Resolution: N = 3 bits
- Code: $2^N = 8$
- Full Scale = 10V
- Voltage step or quantum (Q = FS/N)

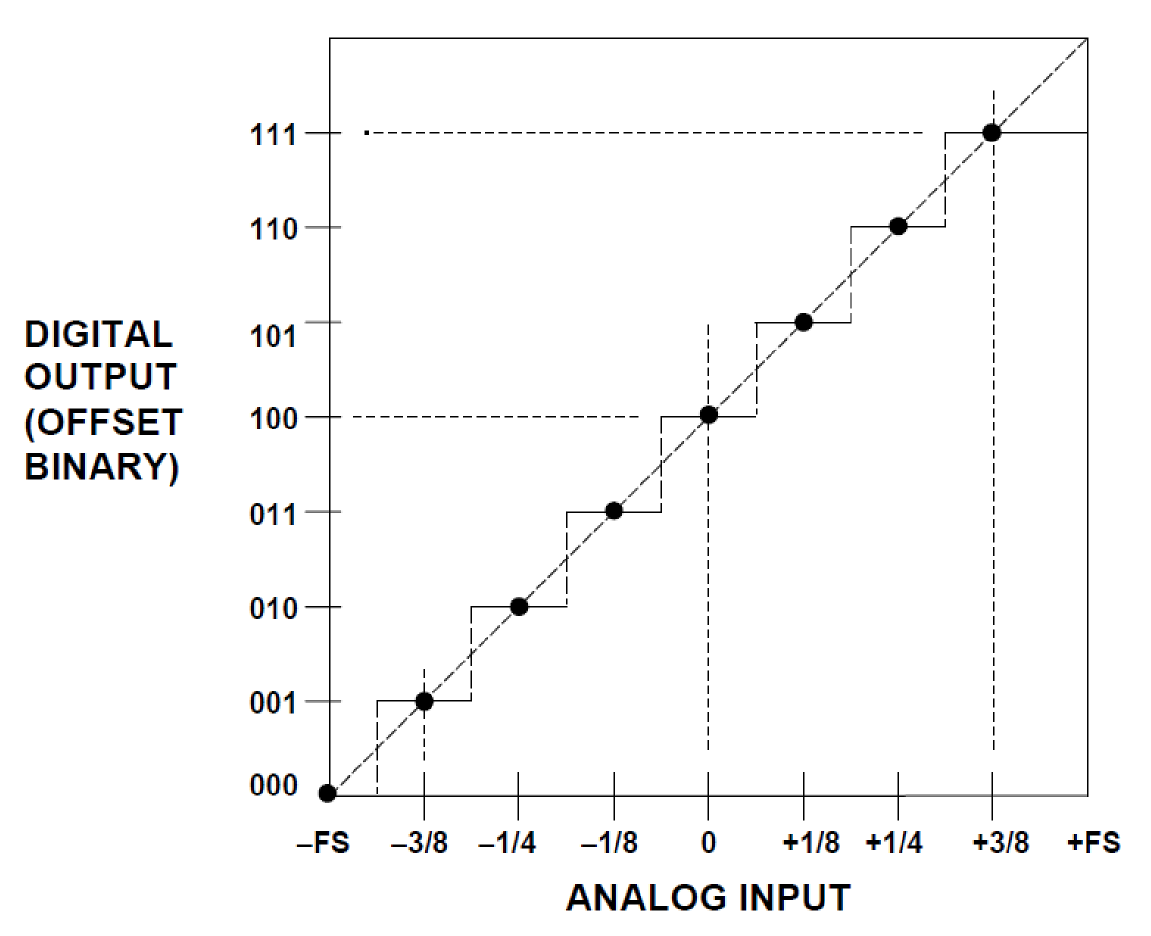
Unipolar Binary Codes

Scale	FS (10V)	Binary
7/8	8,75	111
3/4	7,5	110
5/8	6,25	101
1/2	5	100
3/8	3,75	011
1/4	2,5	010
1/8	1,25	001
0	0	000

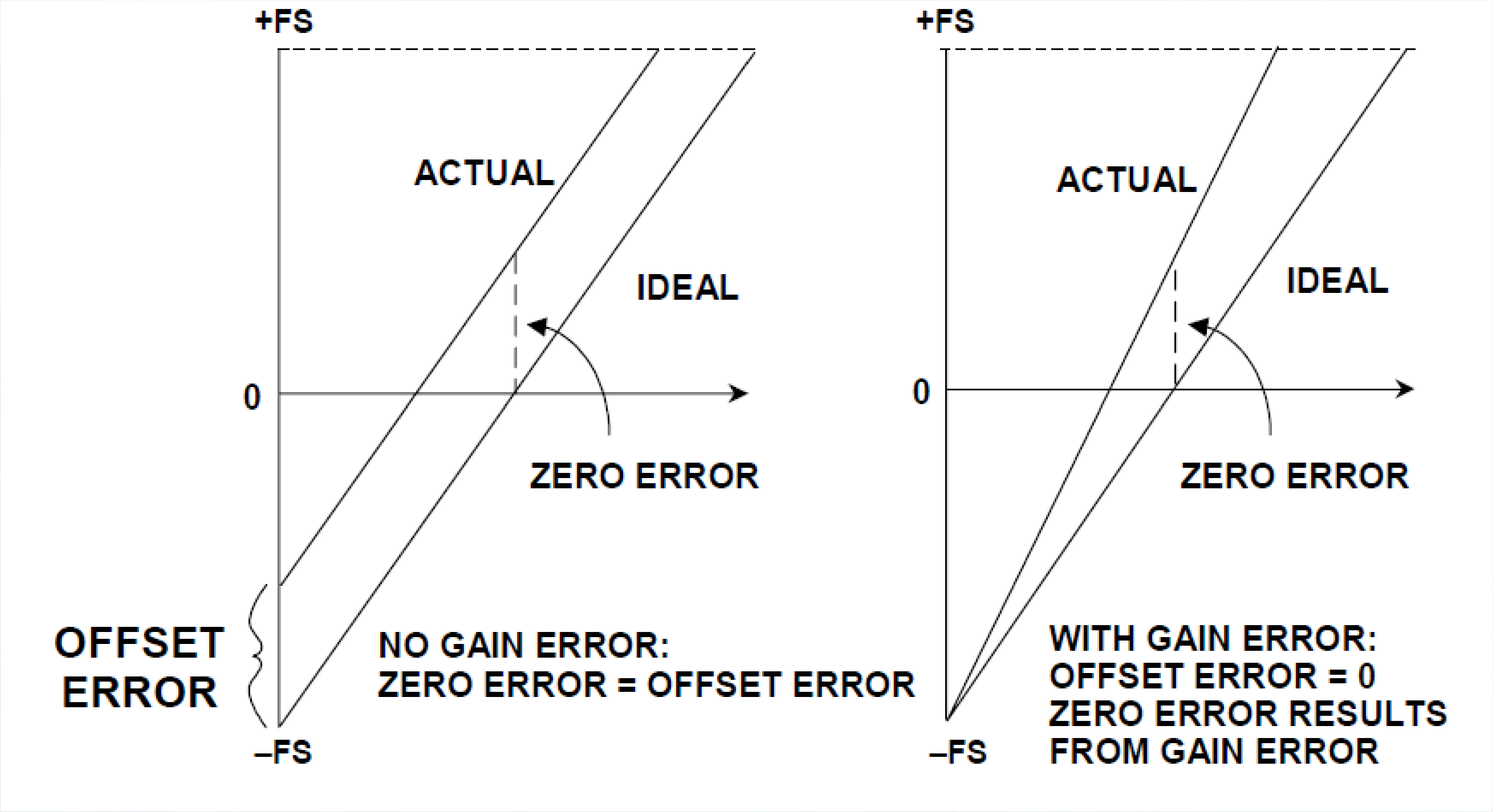


Bipolar Binary Codes

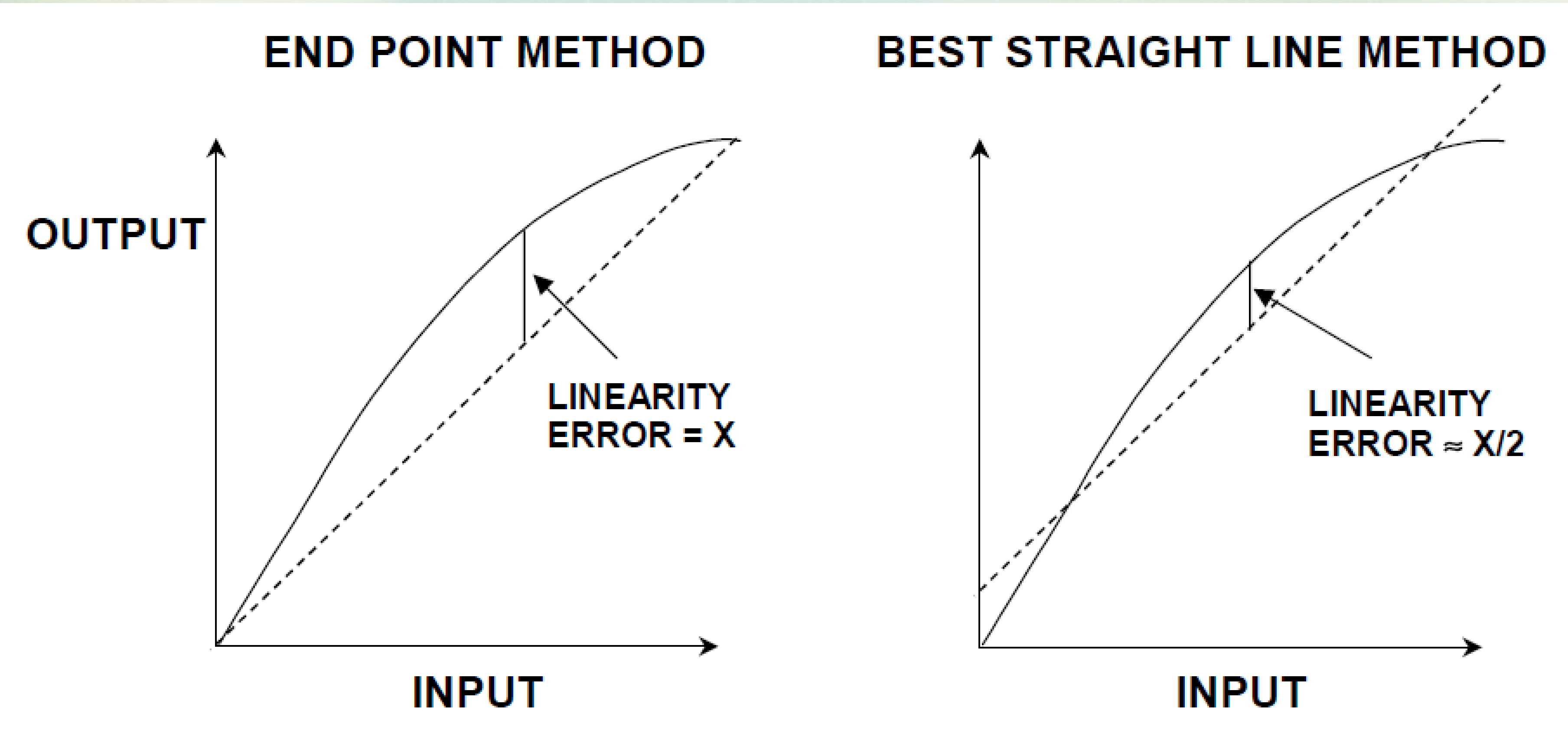
Scale	FS (+/-5V)	Two Comp.
3/4	3,75	011
1/2	2,5	010
1/4	1,25	001
0	0	000
- 1/4	-1,25	111
- 1/2	-2,5	110
- 3/4	-3,75	101
-1	-5	100



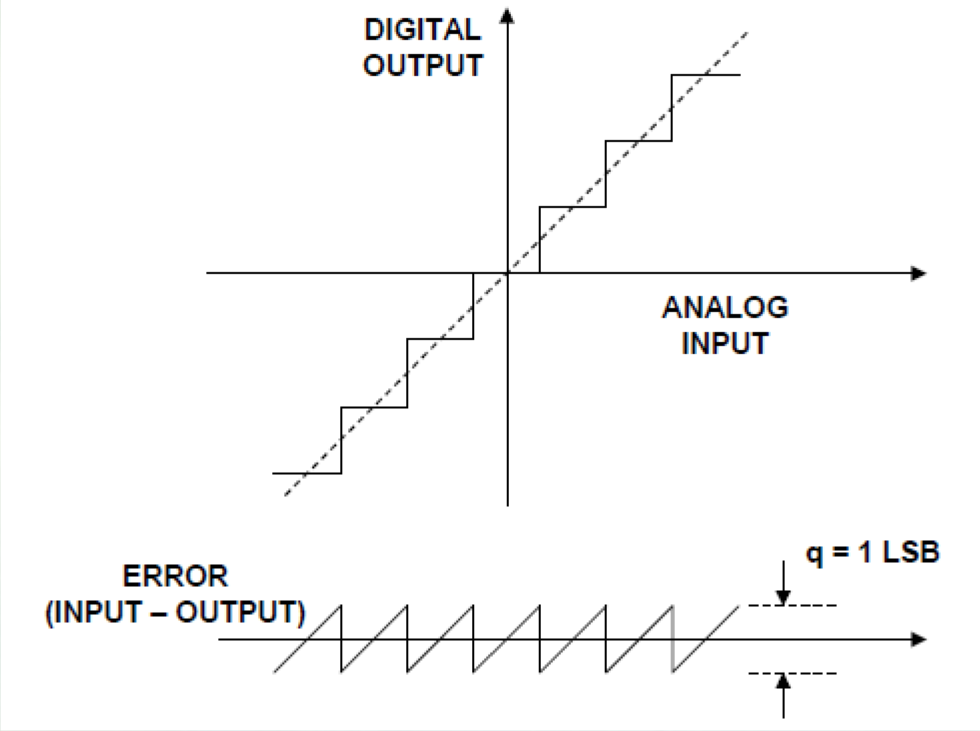
Errors in a data converter

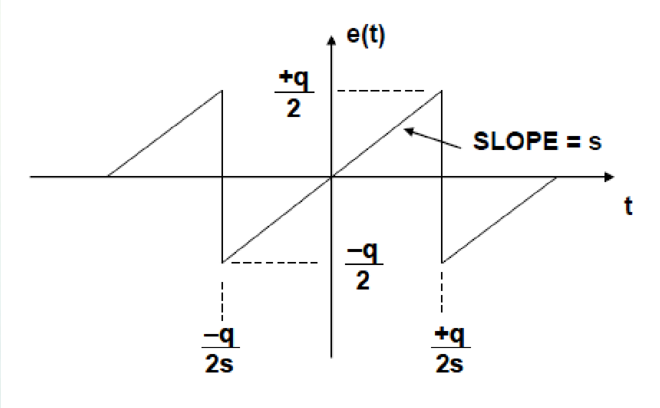


Errors in a data converter



Quantization noise





$$\text{rms quantization noise} = \sqrt{\overline{e^2(t)}} = \frac{q}{\sqrt{12}}.$$

Quantization noise

$$v(t) = \frac{q2^N}{2}\sin(2\pi ft)$$

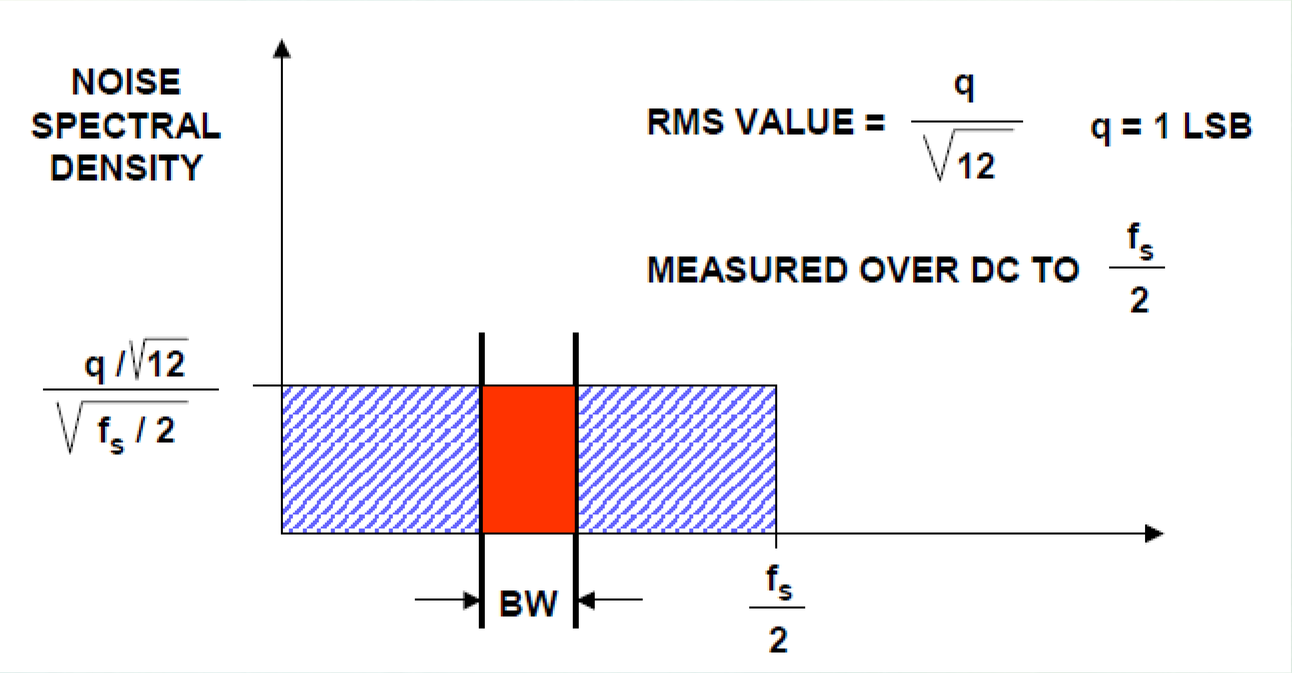
$$v_{rms} = \frac{q2^N}{2\sqrt{2}}$$

$$SNR = 20\log\left(\frac{rms\ value\ of\ input}{rms\ value\ of\ quantization\ noise}\right)$$

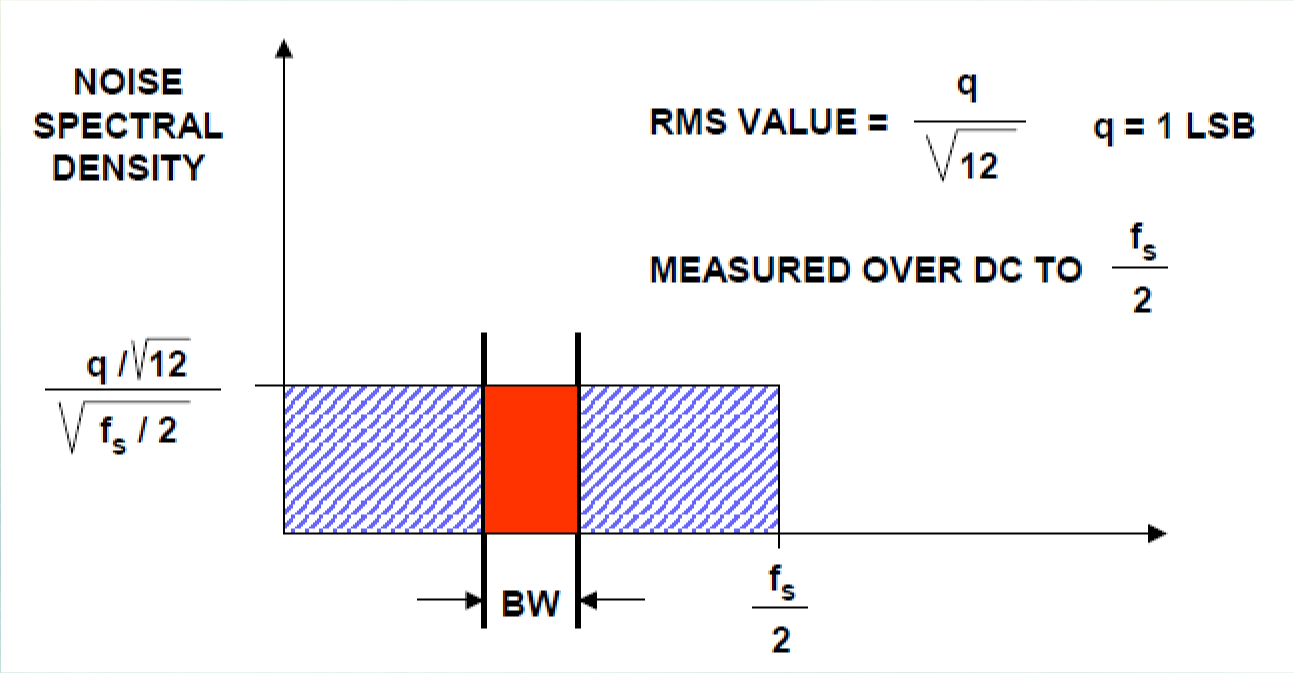
$$SNR = 20\log\left(\frac{\frac{q2^N}{2\sqrt{2}}}{\frac{q}{\sqrt{12}}}\right) = 20\log\left(2^N\right) + 20\log\sqrt{\frac{3}{2}}$$

$$SNR = 6.02N + 1.76dB \quad over\ DC\ to\ \frac{f_s}{2}$$

Quantization noise

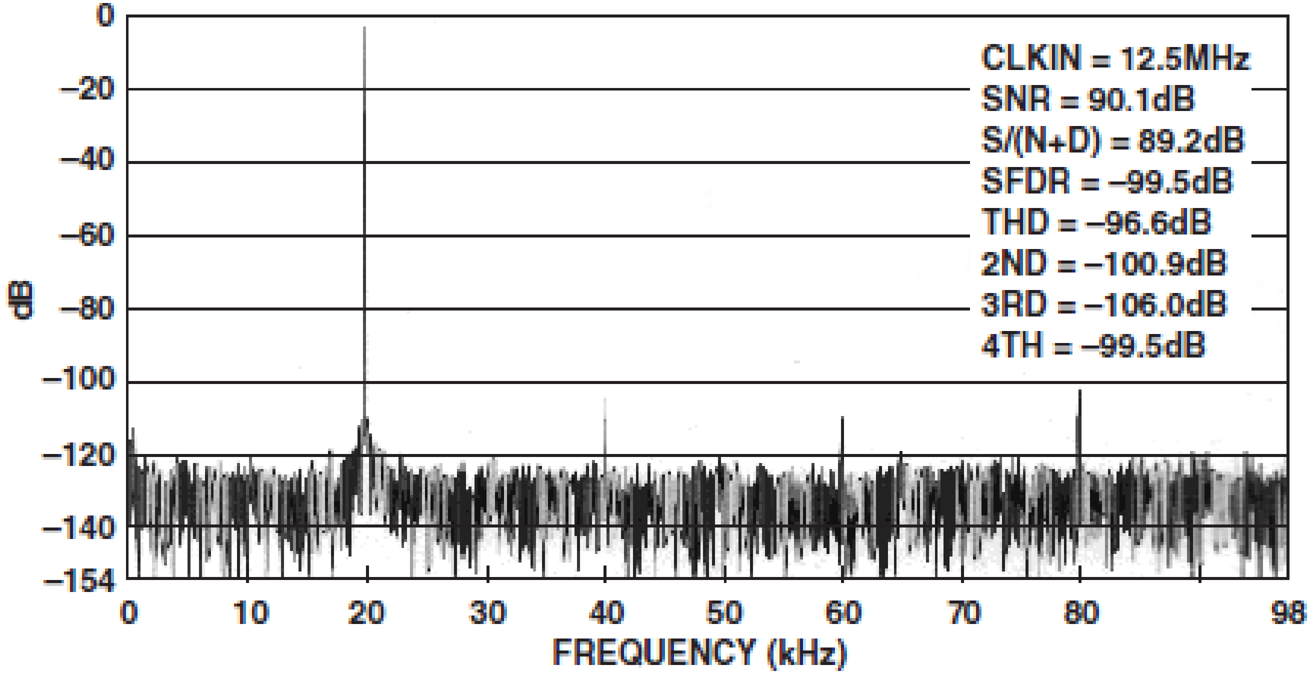


Quantization noise



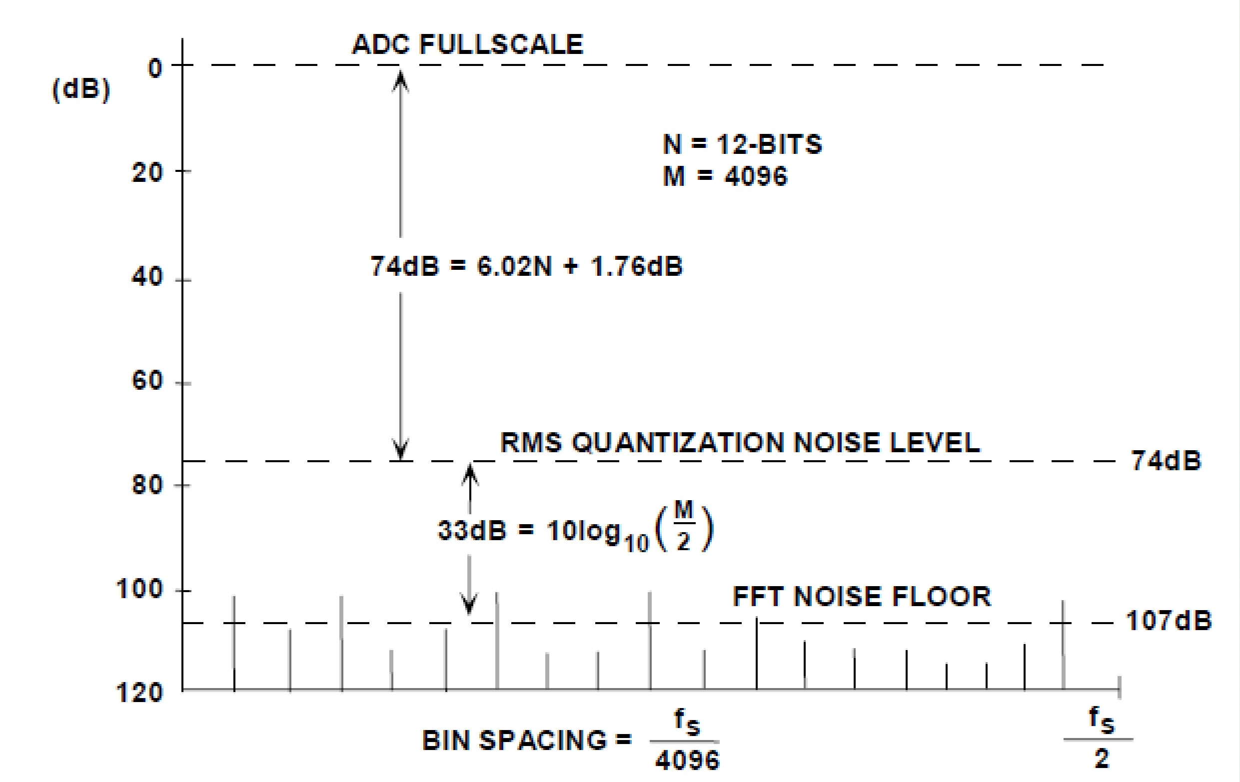
$$SNR = 6.02N + 1.76dB + 10\log\left(\frac{f_s}{2BW}\right)$$

Noise Floor AD7722

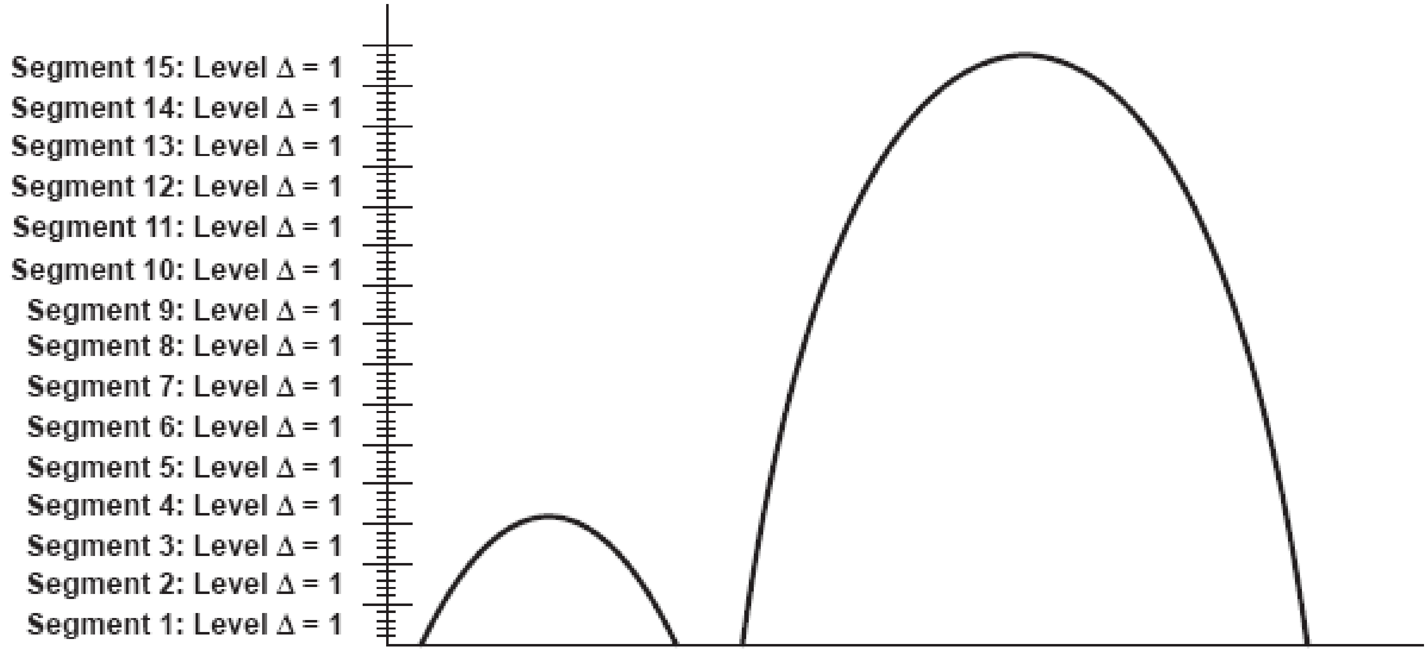


TPC 11. 16K Point FFT

Noise Floor

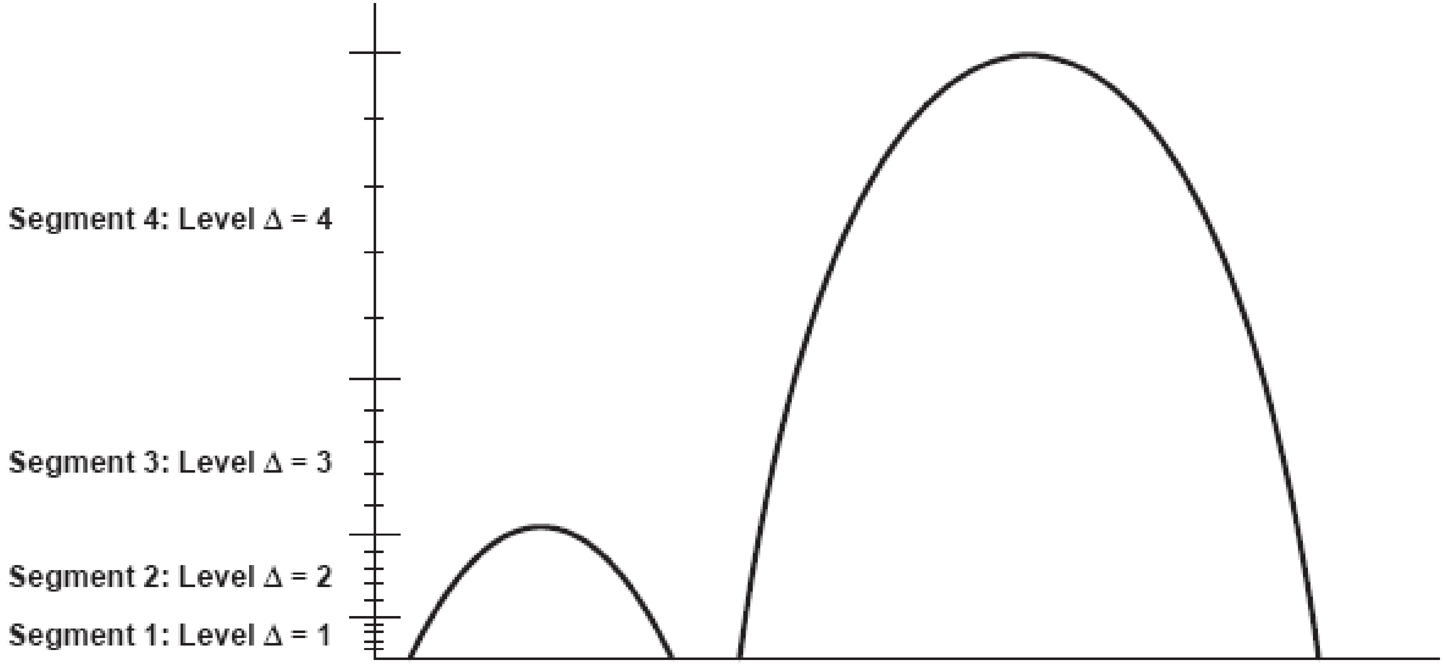

ADC FULLSCALE
(dB)
0
20
40
60
80
100
120
N = 12-BITS
M = 4096
74dB = 6.02N + 1.76dB
RMS QUANTIZATION NOISE LEVEL
74dB
33dB = $10\log_{10}\left(\frac{M}{2}\right)$
FFT NOISE FLOOR
107dB
BIN SPACING = $\frac{f_s}{4096}$
$\frac{f_s}{2}$

Cuantización uniforme



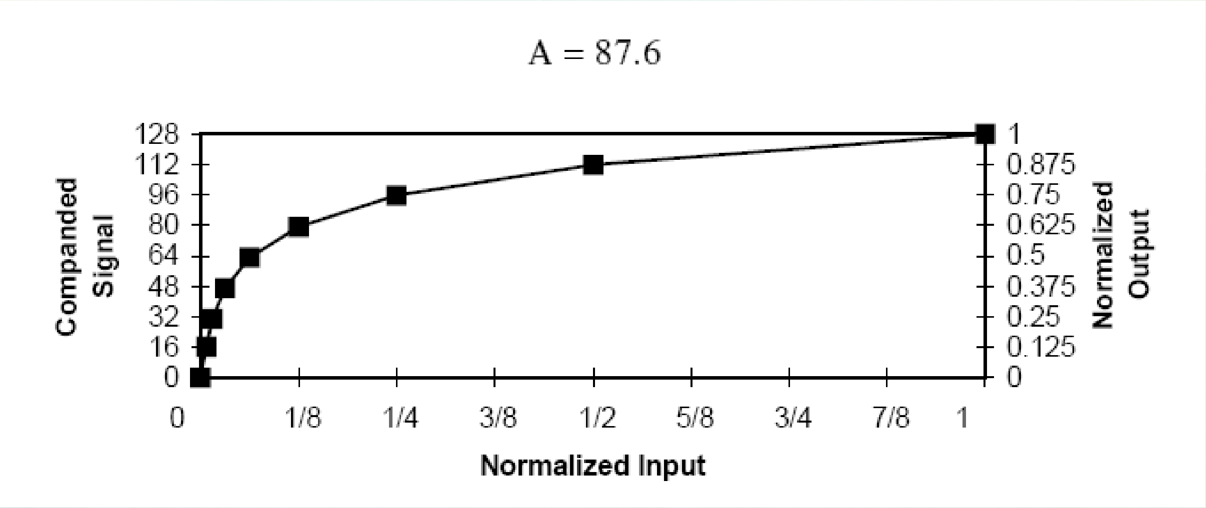
NOTE A: Total number of levels = 75. It requires 7 bits.

Cuantización no uniforme



NOTE A: Total number of levels = 16. It requires 4 bits.

A-law



$$F(x) = \text{sgn}(x)\, A\,|x| \,/\, (1 + \ln A) \qquad 0 \le |x| < 1/A$$
$$\quad = \text{sgn}(x)\, (1+\ln A|x|) \,/\, (1 + \ln A) \qquad 1/A \le |x| \le 1$$

$$DR = 20 \log_{10} (4096/15) = 48.7 \text{ dB}$$

Tabla de codificación

Input Values													Compressed Code Word							
													Chord			Step				
bit:	11	10	9	8	7	6	5	4	3	2	1	0	bit:	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	a	b	c	d	x		0	0	0	a	b	c	d
	0	0	0	0	0	0	1	a	b	c	d	x		0	0	1	a	b	c	d
	0	0	0	0	0	1	a	b	c	d	x	x		0	1	0	a	b	c	d
	0	0	0	0	1	a	b	c	d	x	x	x		0	1	1	a	b	c	d
	0	0	0	1	a	b	c	d	x	x	x	x		1	0	0	a	b	c	d
	0	0	1	a	b	c	d	x	x	x	x	x		1	0	1	a	b	c	d
	0	1	a	b	c	d	x	x	x	x	x	x		1	1	0	a	b	c	d
	1	a	b	c	d	x	x	x	x	x	x	x		1	1	1	a	b	c	d

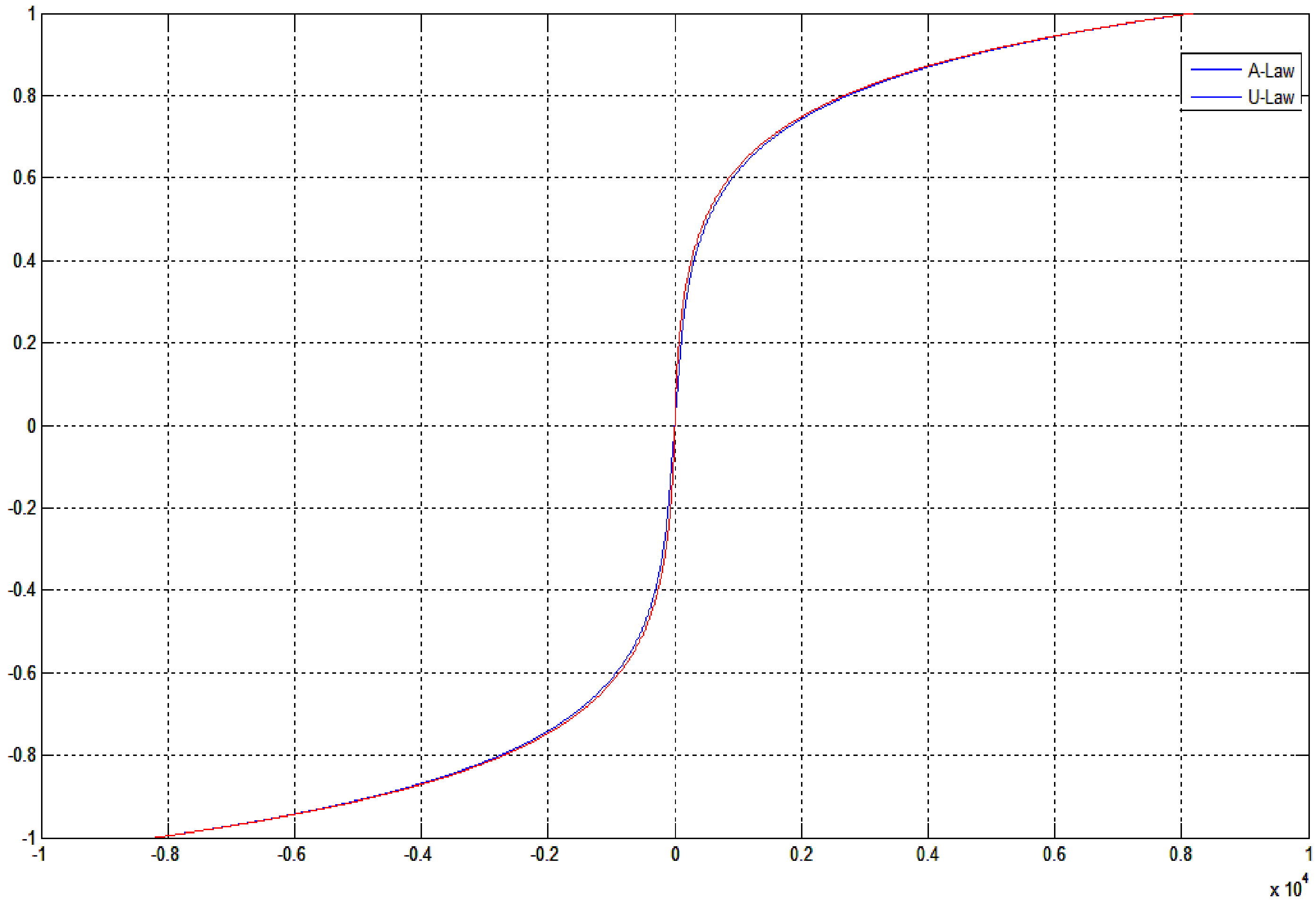
Companding

Integer					A-code			A-code*
-2460_{10}	$= F664_{16}$ $= -99C_{16}$	→	$(1)\ 1001\ 1001\ 1100_2$	→	$(1)\ 111\ 0011_2$	$= F3_{16}$	→	$A6_{16}$
-1505_{10}	$= FA1F_{16}$ $= -5E1_{16}$	→	$(1)\ 0101\ 1110\ 0001_2$	→	$(1)\ 110\ 0111_2$	$= E7_{16}$	→	$B2_{16}$
-650_{10}	$= FD76_{16}$ $= -28A_{16}$	→	$(1)\ 0010\ 1000\ 1010_2$	→	$(1)\ 101\ 0100_2$	$= D4_{16}$	→	81_{16}
-338_{10}	$=FEAE_{16}$ $= -152_{16}$	→	$(1)\ 0001\ 0101\ 0010_2$	→	$(1)\ 100\ 0101_2$	$= C5_{16}$	→	90_{16}
-90_{10}	$= FFA6_{16}$ $= -5A_{16}$	→	$(1)\ 0000\ 0101\ 1010_2$	→	$(1)\ 010\ 0110_2$	$= A6_{16}$	→	$F3_{16}$
-1_{10}	$= FFFF_{16}$ $= -1_{16}$	→	$(1)\ 0000\ 0000\ 0001_2$	→	$(1)\ 000\ 0000_2$	$= 80_{16}$	→	$D5_{16}$
$+40_{10}$	$= 0028_{16}$ $= +28_{16}$	→	$(0)\ 0000\ 0010\ 1000_2$	→	$(0)\ 001\ 0100_2$	$= 14_{16}$	→	41_{16}
$+102_{10}$	$= 0066_{16}$ $= +66_{16}$	→	$(0)\ 0000\ 0110\ 0110_2$	→	$(0)\ 010\ 1001_2$	$= 29_{16}$	→	$7C_{16}$
$+169$	$= 00A9_{16}$ $= +A9_{16}$	→	$(0)\ 0000\ 1010\ 1001_2$	→	$(0)\ 011\ 0101_2$	$= 35_{16}$	→	60_{16}
$+420_{10}$	$= 01A4_{16}$ $= +1A4_{16}$	→	$(0)\ 0001\ 1010\ 0100_2$	→	$(0)\ 100\ 1010_2$	$= 4A_{16}$	→	$1F_{16}$
$+499_{10}$	$= 01F3_{16}$ $= +1F3_{16}$	→	$(0)\ 0001\ 1111\ 0011_2$	→	$(0)\ 100\ 1111_2$	$= 4F_{16}$	→	$1A_{16}$
$+980_{10}$	$= 03D4_{16}$ $= +3D4_{16}$	→	$(0)\ 0011\ 1101\ 0100_2$	→	$(0)\ 101\ 1110_2$	$= 5E_{16}$	→	$0B_{16}$

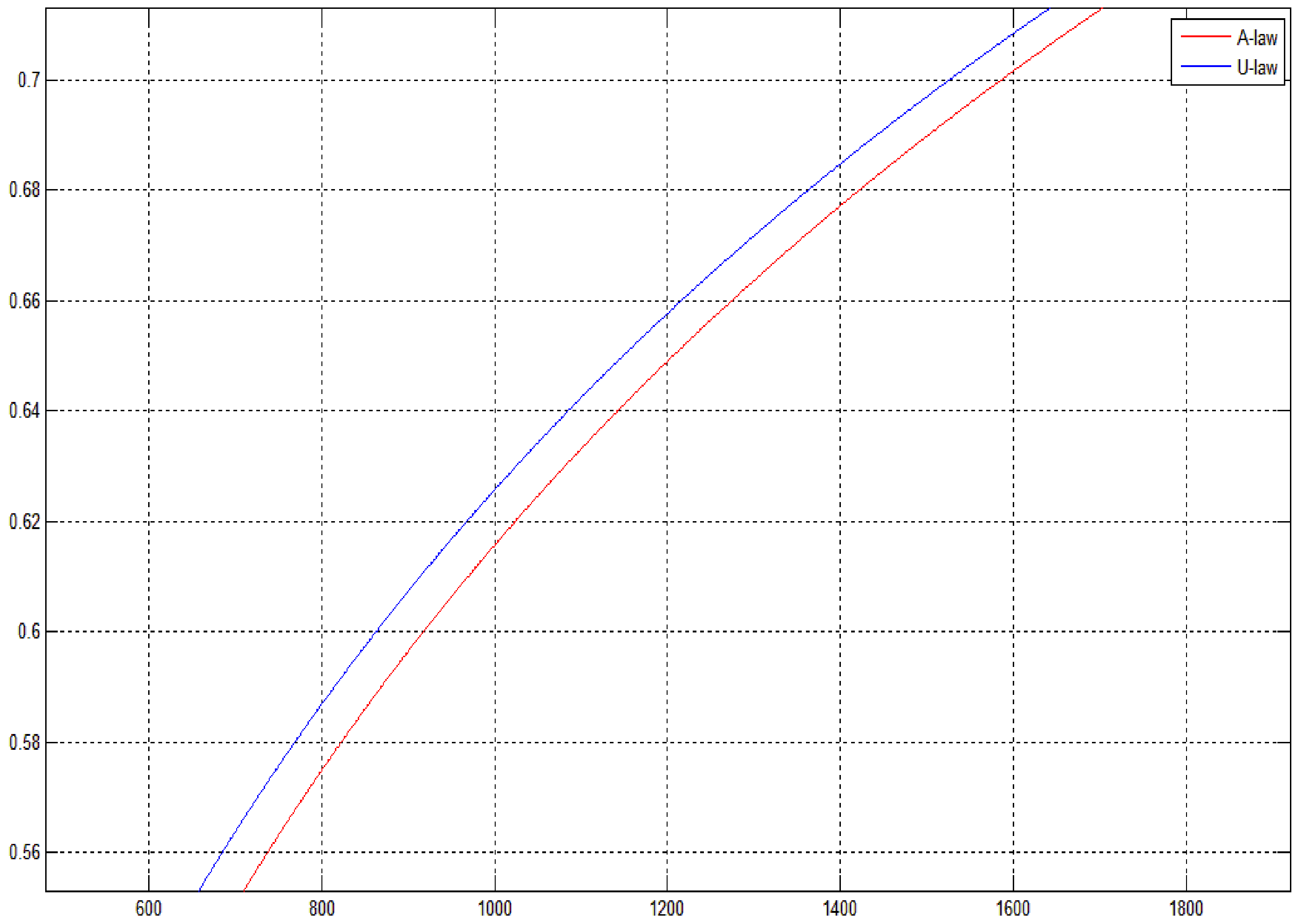
Expansion

A-code*		A-code				Expanded Integer		
$A6_{16}$	→	$F3_{16}$	=	$(1)\ 111\ 0011_2$	→	$(1)\ 1001\ 1100\ 0000_2$	→	$-9C0_{16} = -2496_{10}$ $= F640_{16}$
$B2_{16}$	→	$E7_{16}$	=	$(1)\ 110\ 0111_2$	→	$(1)\ 0101\ 1110\ 0000_2$	→	$-5E0_{16} = -1504_{10}$ $= FA20_{16}$
81_{16}	→	$D4_{16}$	=	$(1)\ 101\ 0100_2$	→	$(1)\ 0010\ 1001\ 0000_2$	→	$-290_{16} = -656_{10}$ $= FD70_{16}$
90_{16}	→	$C5_{16}$	=	$(1)\ 100\ 0101_2$	→	$(1)\ 0001\ 0101\ 1000_2$	→	$-158_{16} = -344_{10}$ $= FEA8_{16}$
$F3_{16}$	→	$A6_{16}$	=	$(1)\ 010\ 0110_2$	→	$(1)\ 0000\ 0101\ 1010_2$	→	$-5A_{16} = -90_{10}$ $= FFA6_{16}$
$D5_{16}$	→	80_{16}	=	$(1)\ 000\ 0000_2$	→	$(1)\ 0000\ 0000\ 0001_2$	→	$-1_{16} = -1_{10}$ $= FFFF_{16}$
41_{16}	→	14_{16}	=	$(0)\ 001\ 0100_2$	→	$(0)\ 0000\ 0010\ 1001_2$	→	$+29_{16} = +41_{10}$ $= 0029_{16}$
$7C_{16}$	→	29_{16}	=	$(0)\ 010\ 1001_2$	→	$(0)\ 0000\ 0110\ 0110_2$	→	$+66_{16} = +102_{10}$ $= 0066_{16}$
60_{16}	→	35_{16}	=	$(0)\ 011\ 0101_2$	→	$(0)\ 0000\ 1010\ 1100_2$	→	$+AC_{16} = +172_{10}$ $= 00AC_{16}$
$1F_{16}$	→	$4A_{16}$	=	$(0)\ 100\ 1010_2$	→	$(0)\ 0001\ 1010\ 1000_2$	→	$+1A8_{16} = +424_{10}$ $= 01A8_{16}$
$1A_{16}$	→	$4F_{16}$	=	$(0)\ 100\ 1111_2$	→	$(0)\ 0001\ 1111\ 1000_2$	→	$+1F8_{16} = +504_{10}$ $= 01F8_{16}$
$0B_{16}$	→	$5E_{16}$	=	$(0)\ 101\ 1110_2$	→	$(0)\ 0011\ 1101\ 0000_2$	→	$+3D0_{16} = +976_{10}$ $= 03D0_{16}$

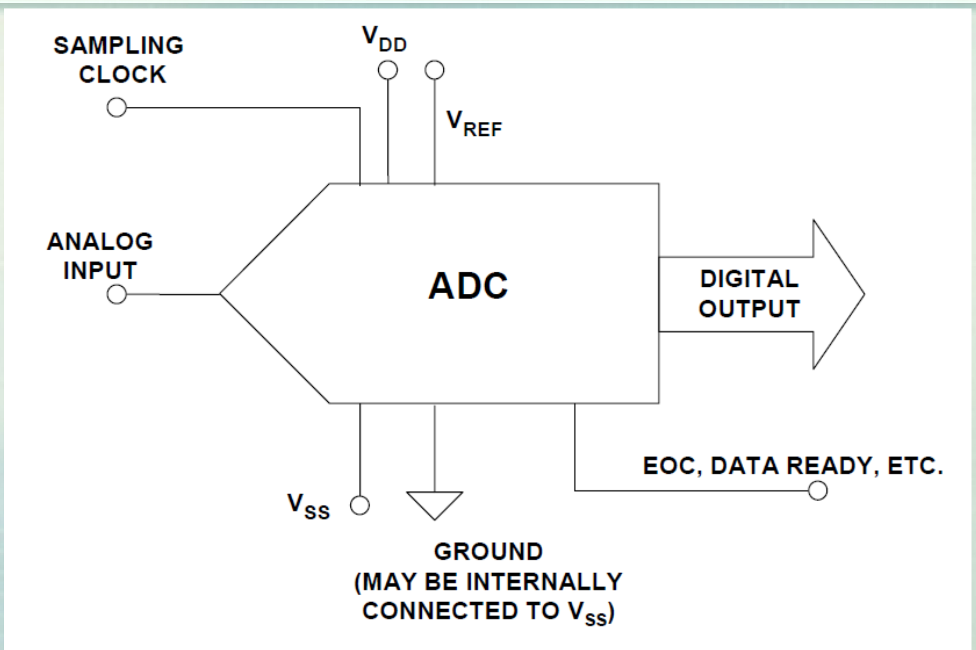
Differences Between A–Law and u–Law



Differences Between A–Law and u–Law



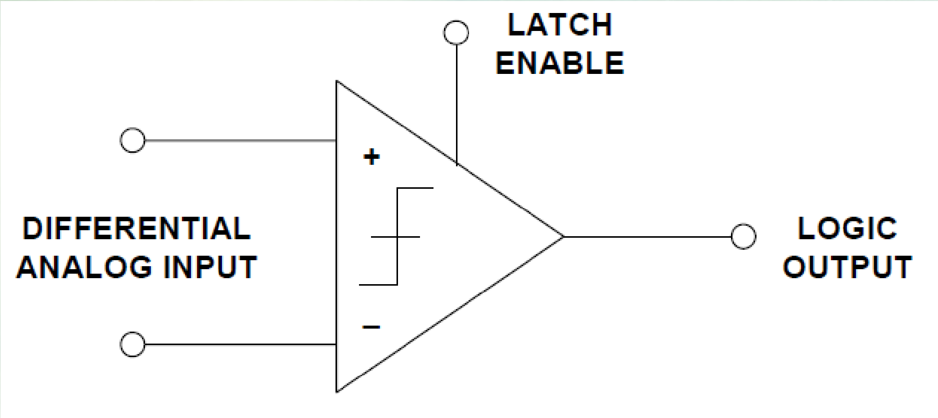
Basic ADC

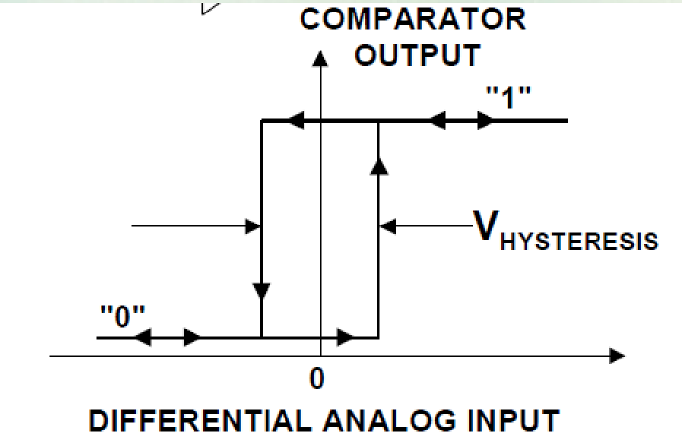


Analog:
- Analog Input
- Reference Voltage
- Analog Ground
- Analog Power Supply

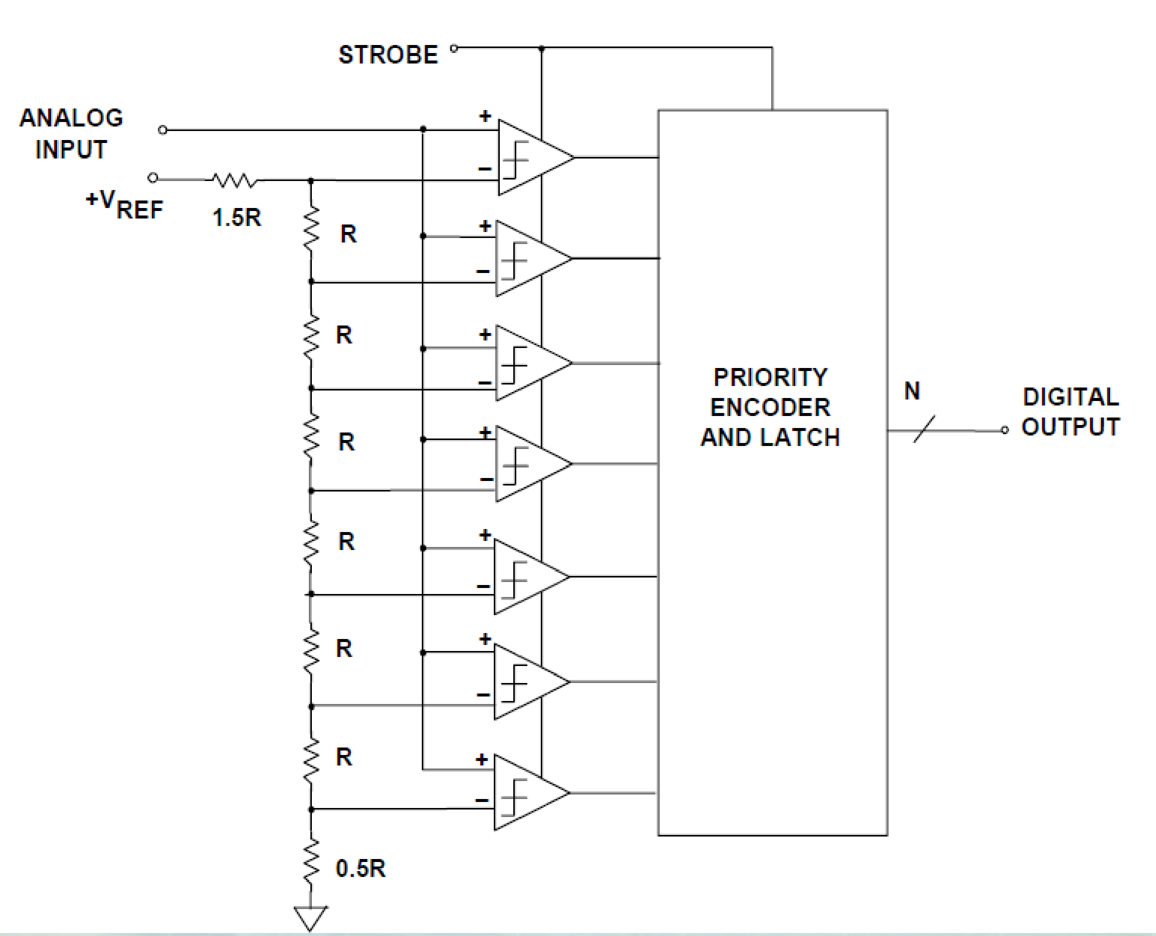
Digital:
- Digital output
- Control Signals
- Sampling Clock
- Digital Ground
- Digital Power Supply

1-Bit DAC


LATCH
ENABLE
+
−
DIFFERENTIAL
ANALOG INPUT
LOGIC
OUTPUT

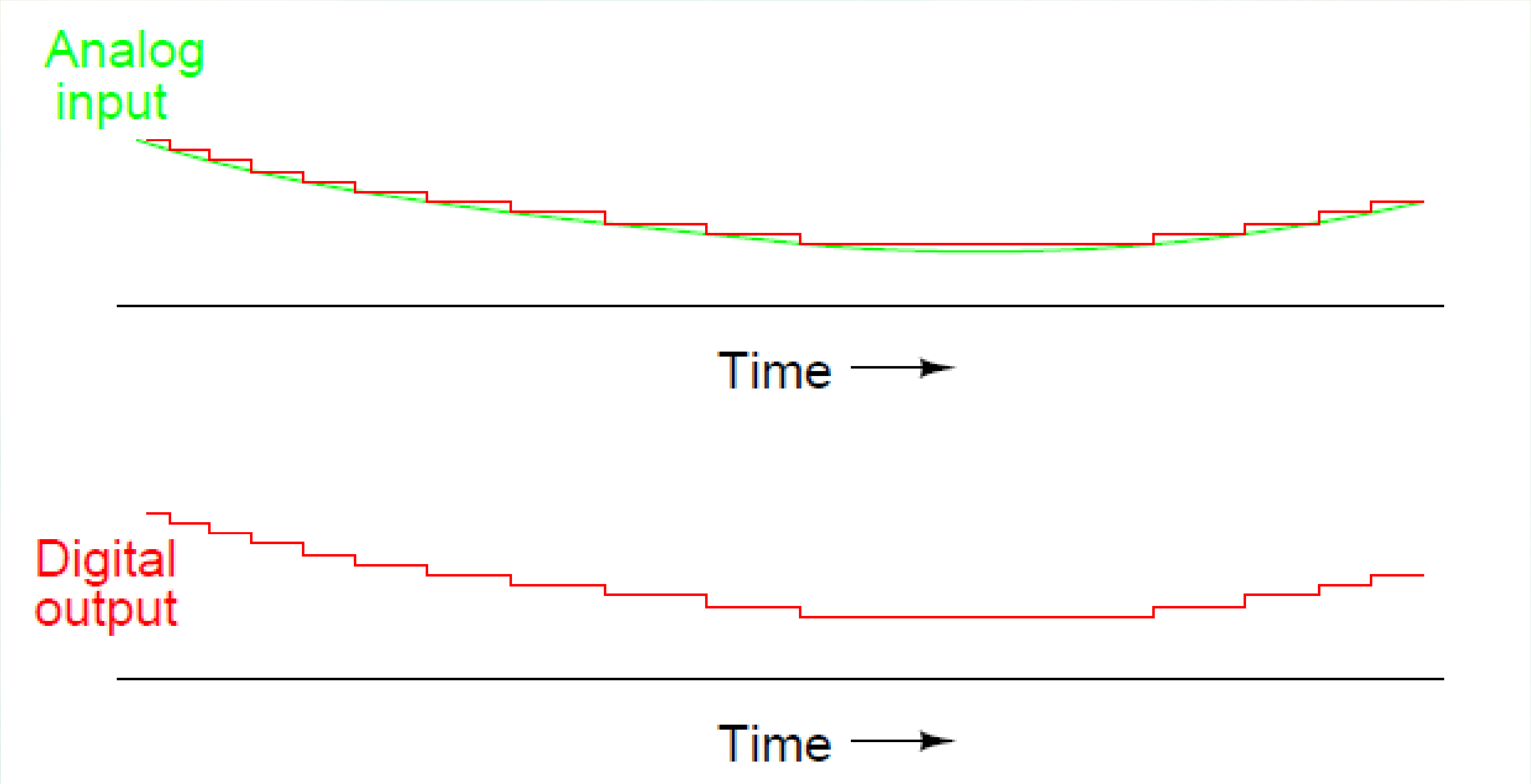

COMPARATOR
OUTPUT
"1"
$V_{HYSTERESIS}$
"0"
0
DIFFERENTIAL ANALOG INPUT

Flash converters

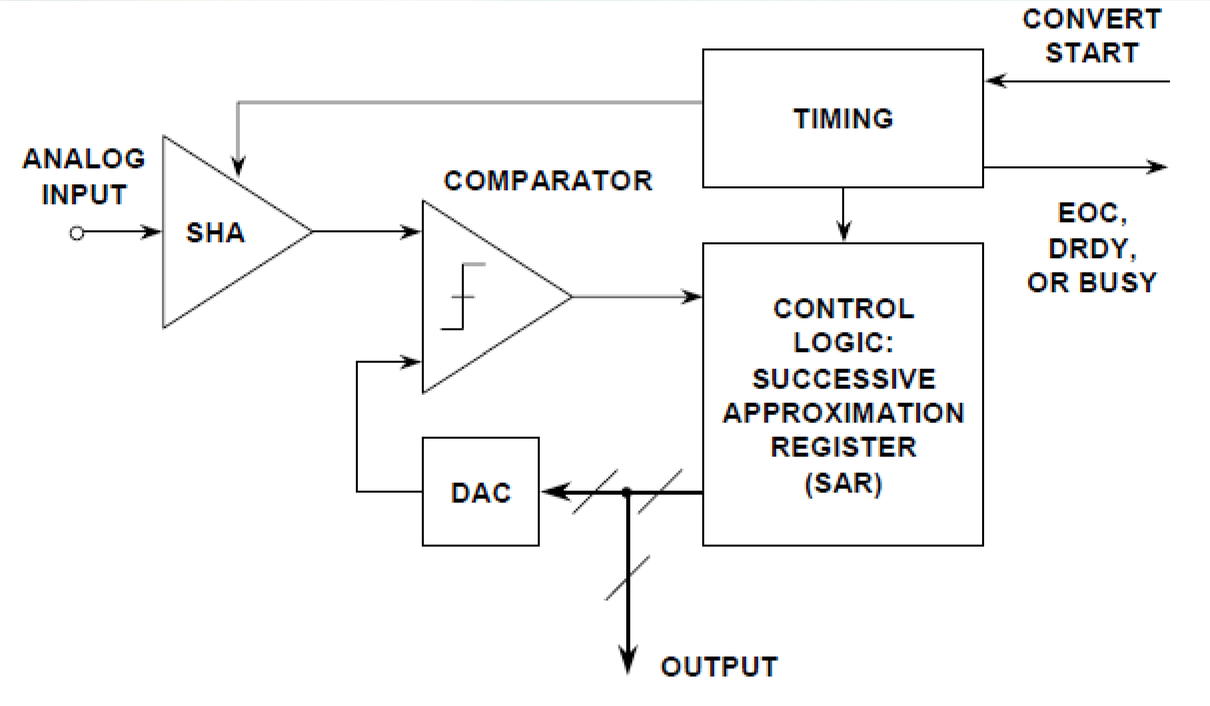


- Expensives
- High power
- Resolution limited to around 8-bits
- Large chip size
- Fast
- Resistors: 2^N
- Comparators: $2^{(N-1)}$

Flash converters

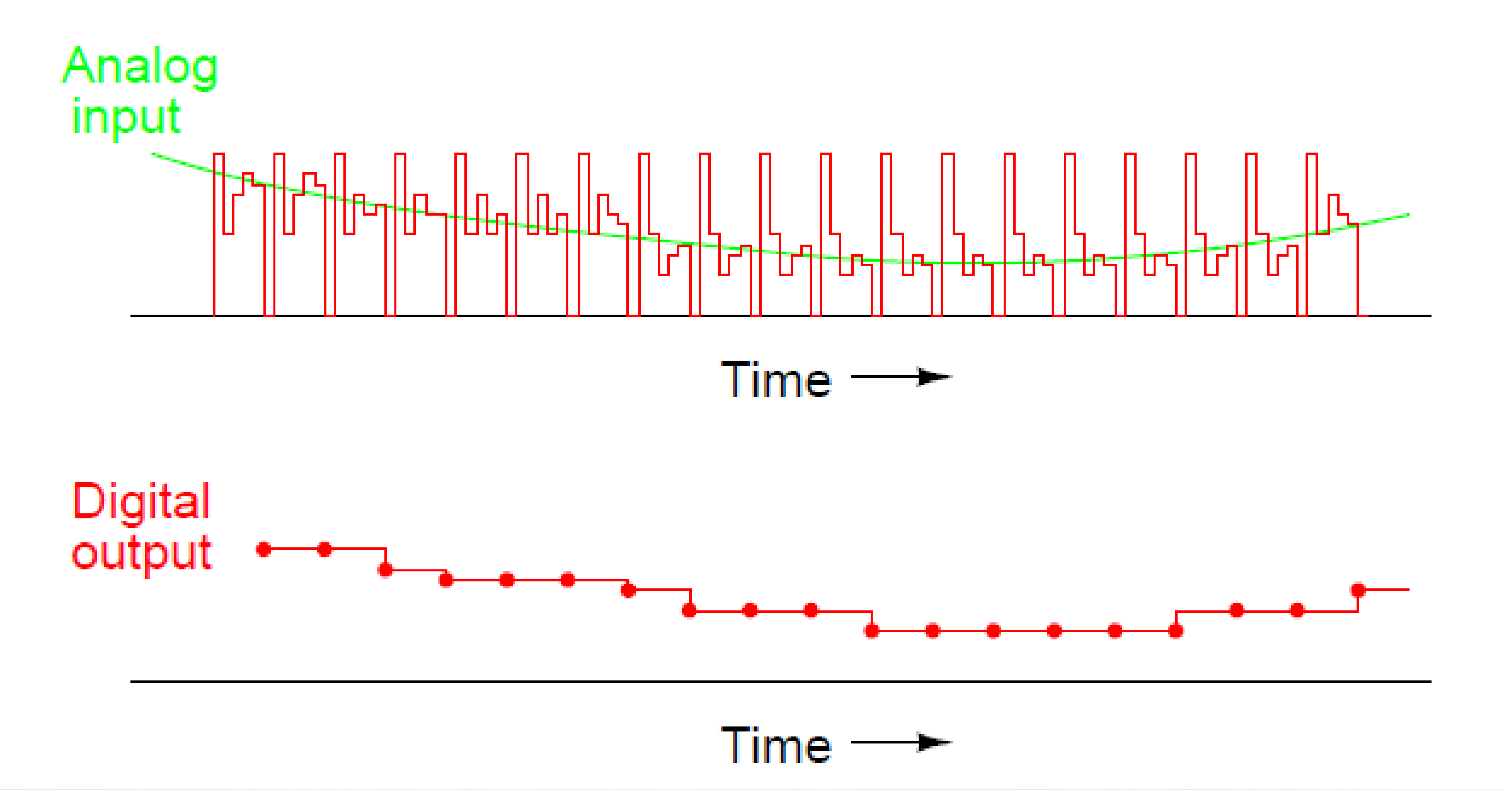


SAR

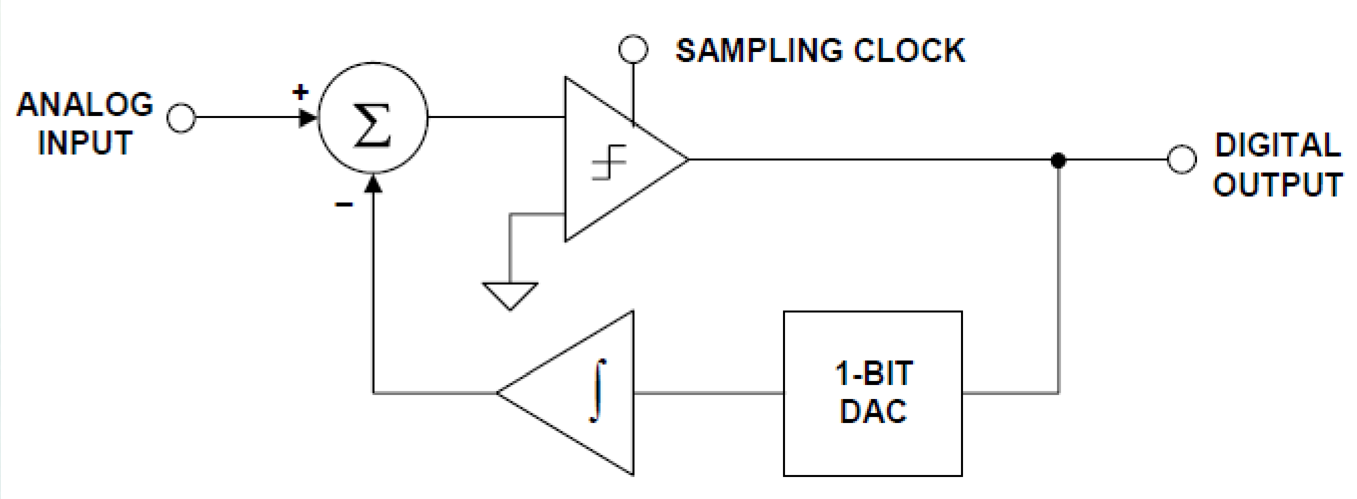


- The accuracy and linearity is determined by the DAC
- Available in resolutions up to 16-bits

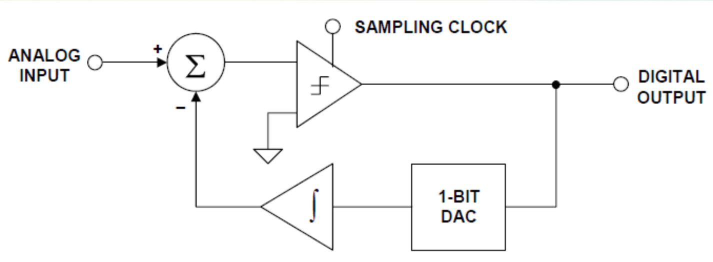
SAR

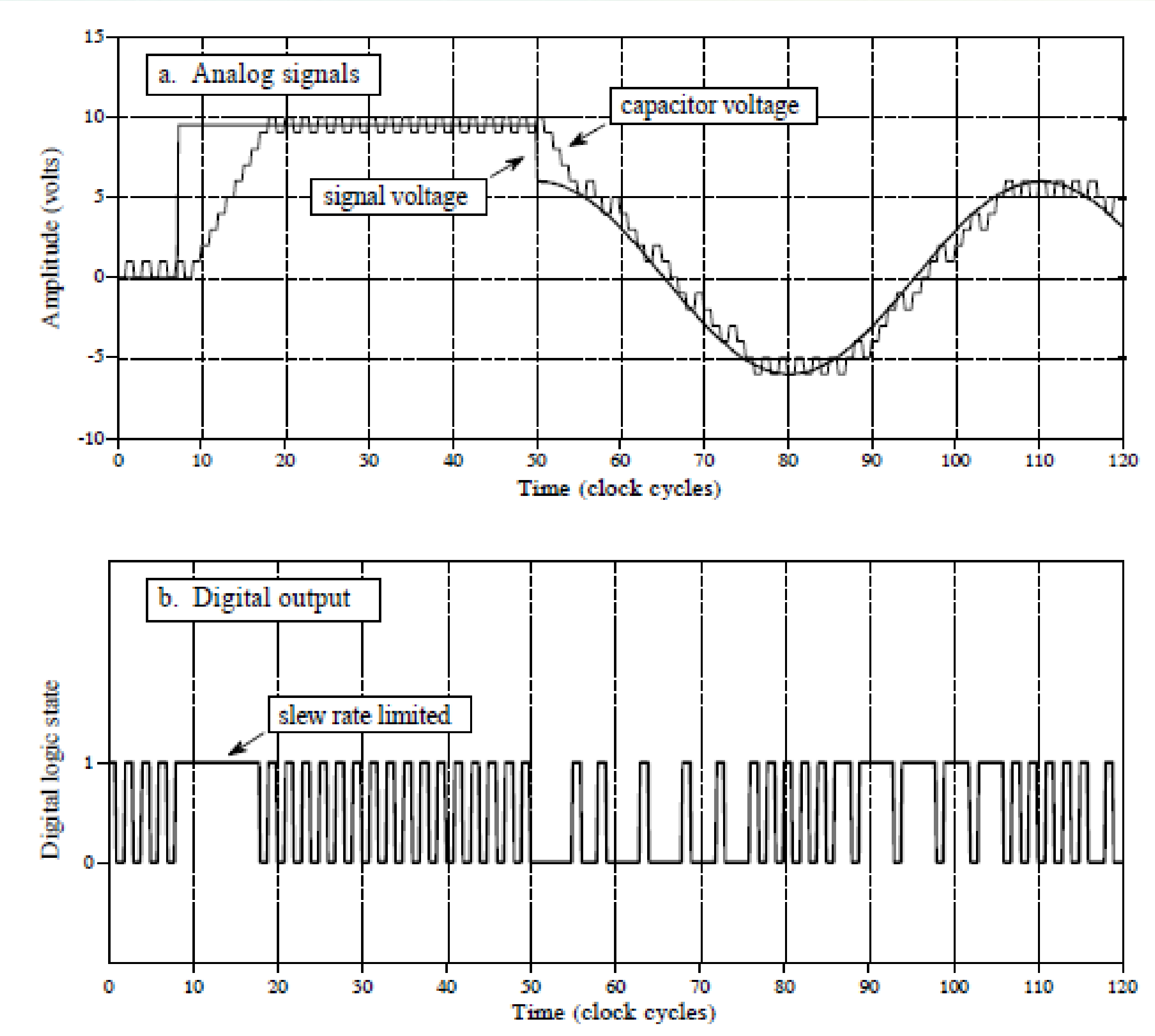


Delta Modulation

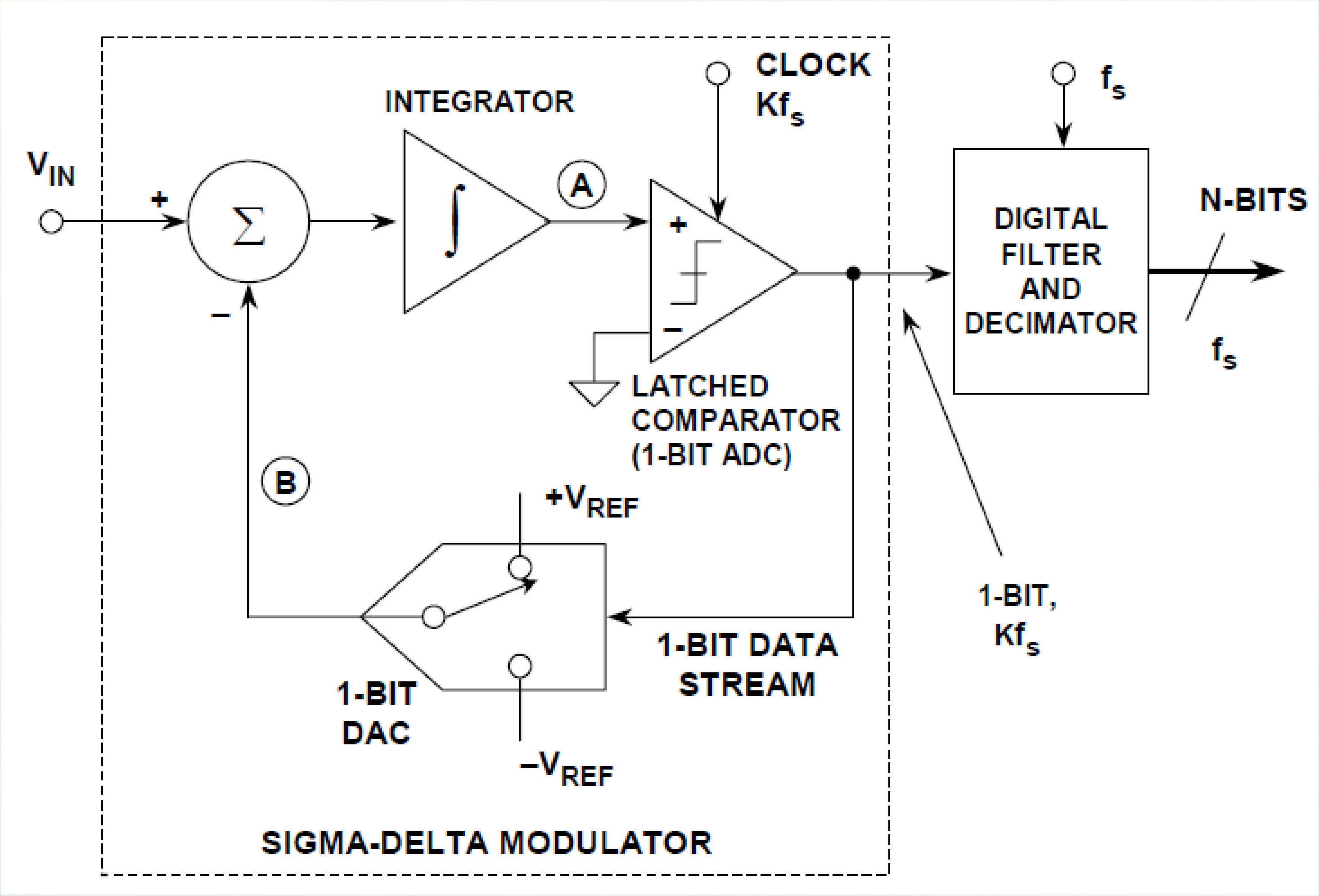


Delta Modulation

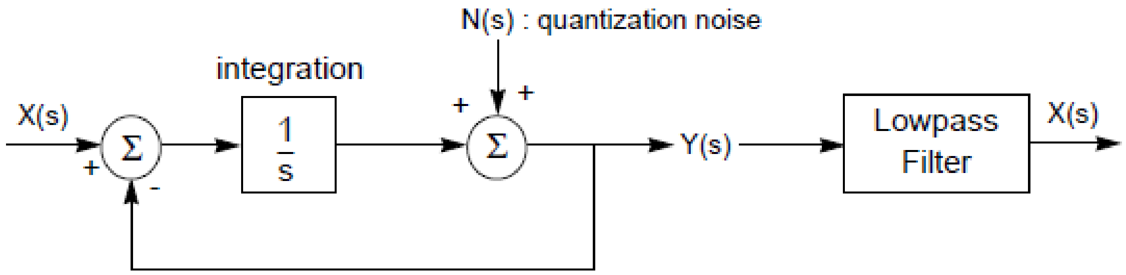




First-Order Sigma-Delta ADC



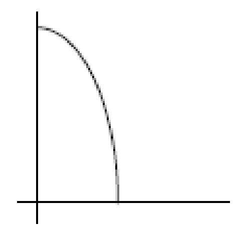
Analysis of Sigma-Delta Modulator



Signal Transfer Function: (when N(s) = 0)

$$Y(s) = [X(s) - Y(s)]\ \frac{1}{s}$$

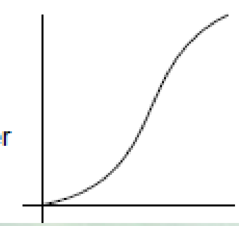
$$\frac{Y(s)}{X(s)} = \frac{\frac{1}{s}}{1 + \frac{1}{s}} = \frac{1}{s+1}$$: lowpass filter



Noise Transfer Function: (when X(s) = 0)

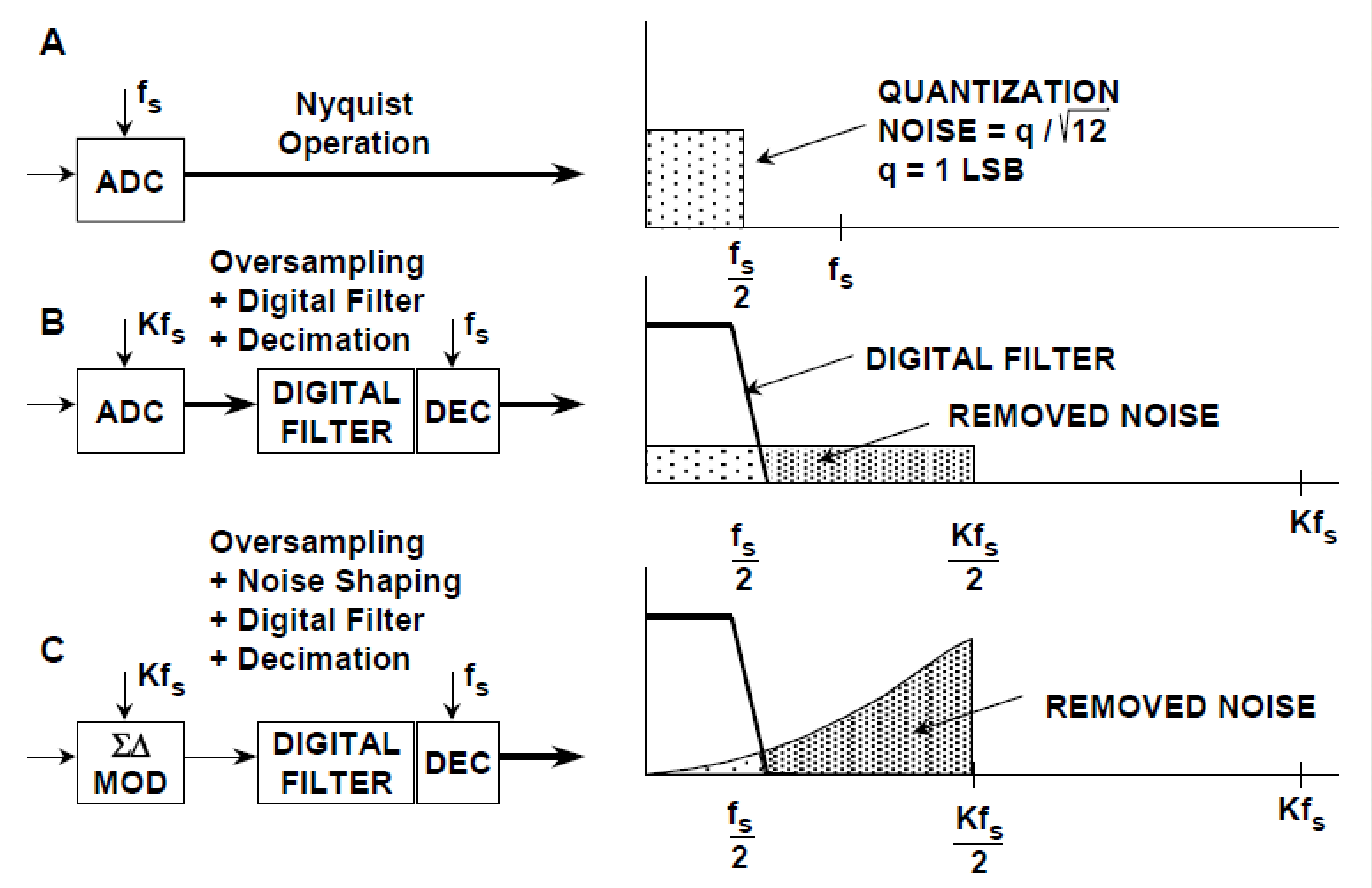
$$Y(s) = -Y(s)\frac{1}{s} + N(s)$$

$$\frac{Y(s)}{N(s)} = \frac{1}{1 + \frac{1}{s}} = \frac{s}{s+1}$$: highpass filter

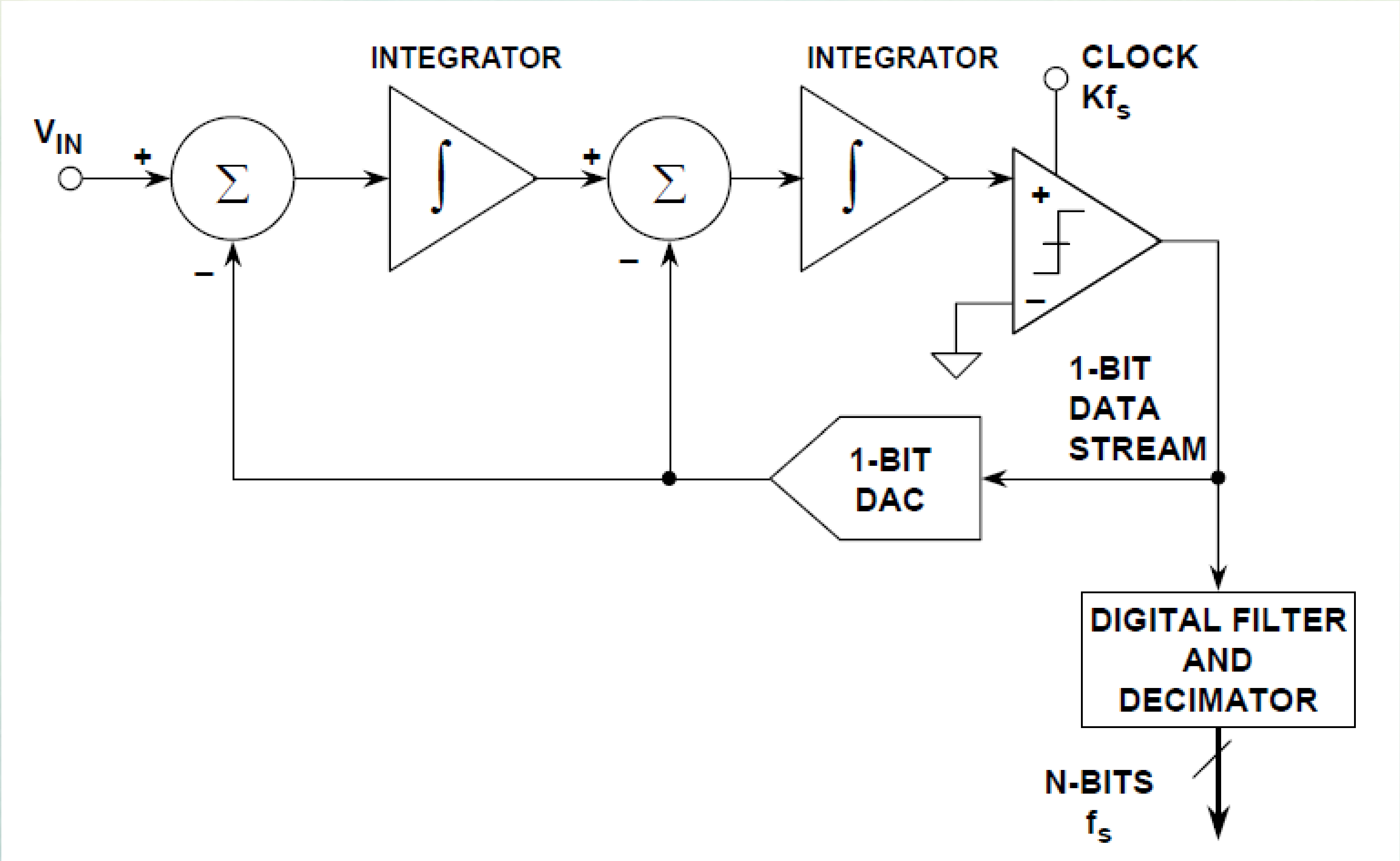


- The integrator acts as a lowpass filter to the input signal and a highpass filter to the quantization noise

Oversampling



Second-Order Sigma-Delta ADC



Architecture tradeoffs