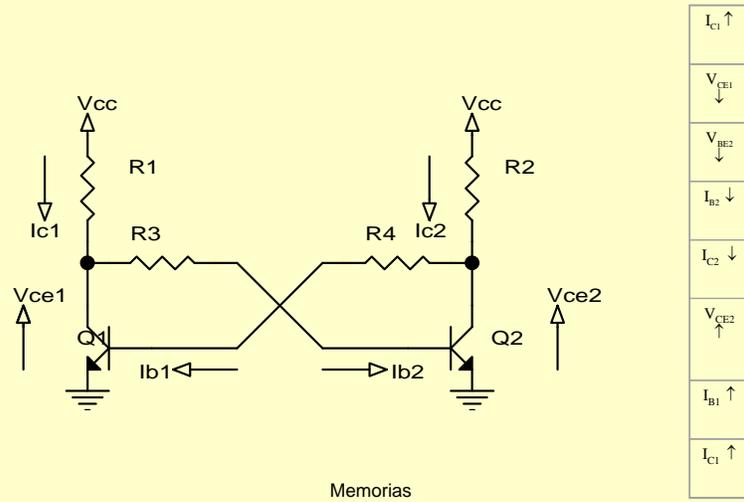
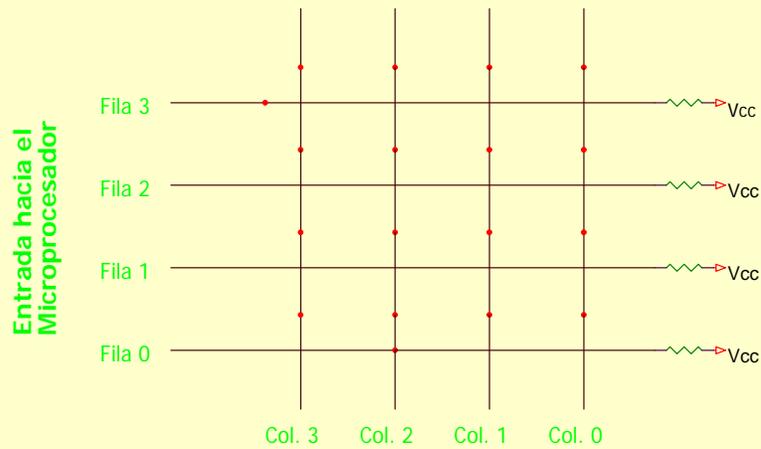


## Principios de funcionamiento.



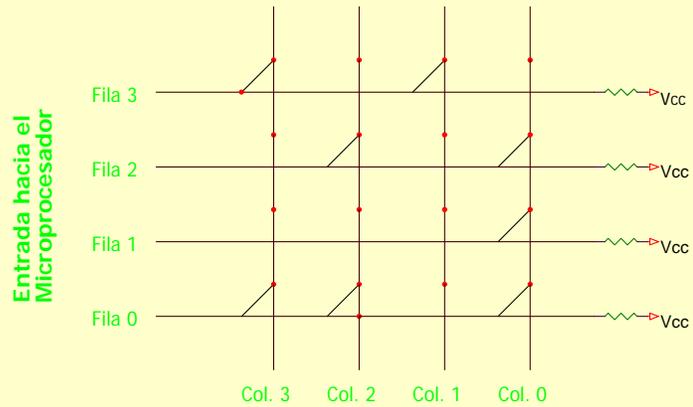
1

## Almacenamiento de información binaria



2

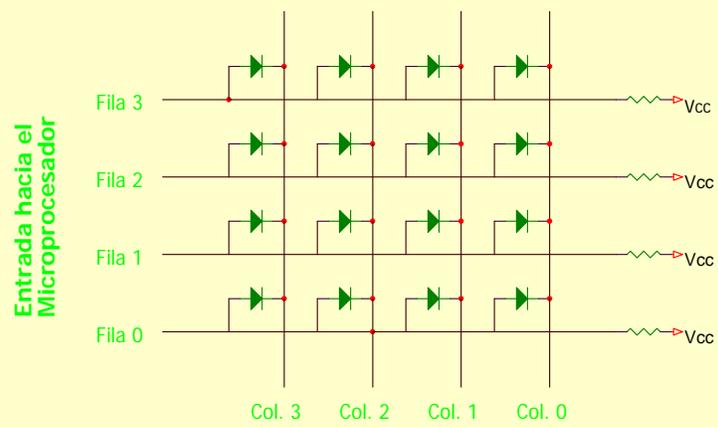
## Cableado de uniones



Memorias

3

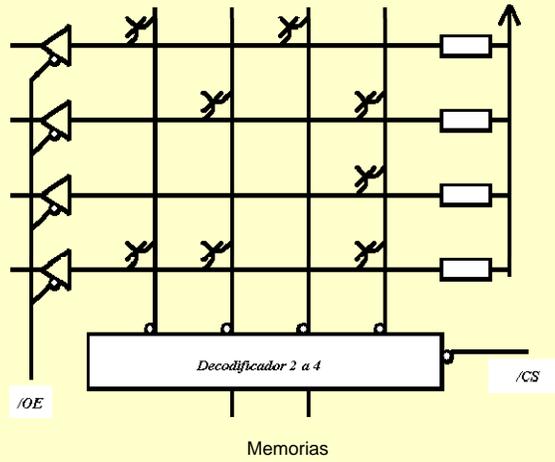
## Uso de Diodos



Memorias

4

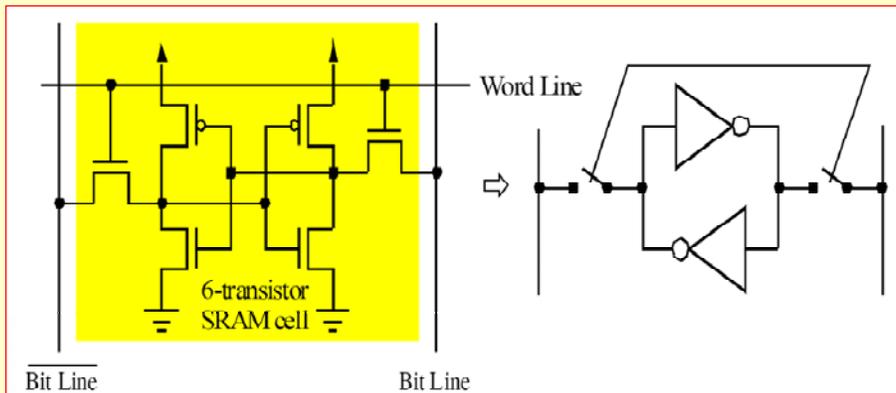
## Uso de transistores



Memorias

5

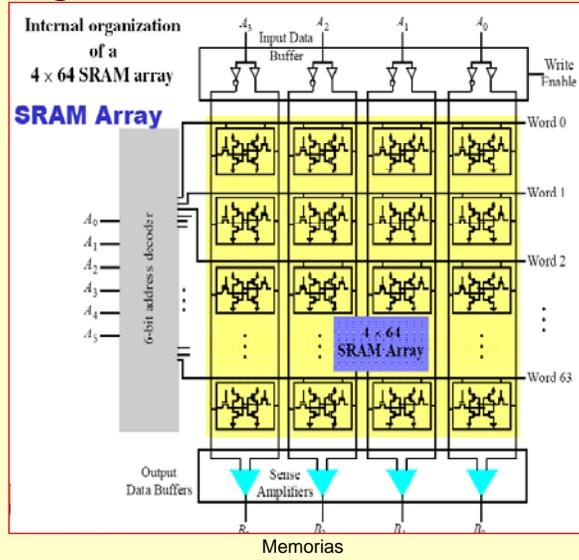
## Implementación en MOS



Memorias

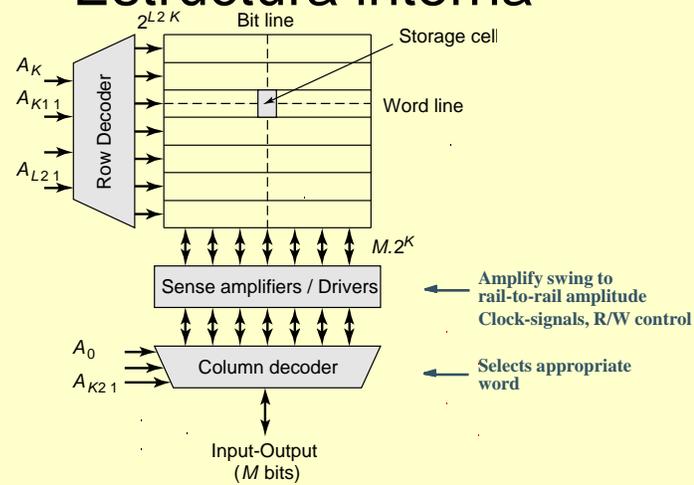
6

# Diagrama de una memoria



7

# Estructura interna



Memorias

8

# Memorias

- Los programas SIEMPRE se ejecutan en la memoria semiconductora.
- La memoria magnética es muy barata por bit, pero muy lenta.

# Clasificación de las memorias

De lectura - escritura <i>Volátiles</i>		De Lectura mayoritaria <i>No-Volátiles</i>	De lectura solamente <i>No-Volátiles</i>
<b>Acceso Aleatorio</b>	<b>Acceso Secuencial</b>	EPROM E <sup>2</sup> PROM FLASH	De máscara Programable (PROM)
SRAM DRAM	FIFO LIFO Shift Register CAM		

## Clasificación.

### *Según su funcionamiento*

Memorias Estáticas.

Memorias Dinámicas.

### *Según su persistencia*

Memorias volátiles

Memorias Perennes.

Memorias

11

## Clasificación

### *Según su tecnología.*

- PMOS.
- NMOS.
- CMOS
- HMOS
- HCMOS

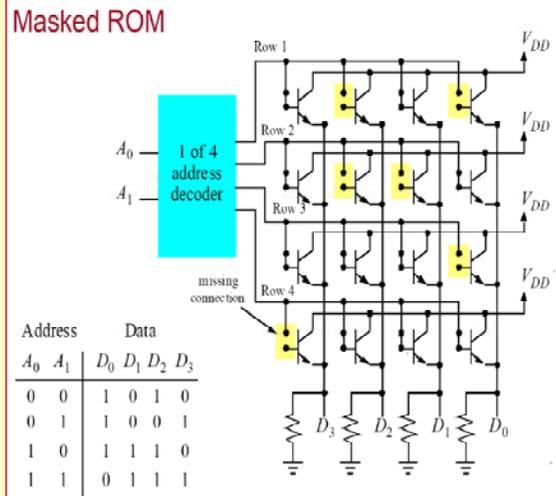
### *Según su uso.*

- De lectura y escritura.
- De lectura solamente.

Memorias

12

# ROMs de máscara

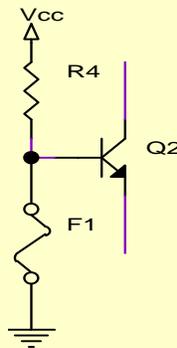


Memorias

13

# Memorias de Lectura mayoritaria

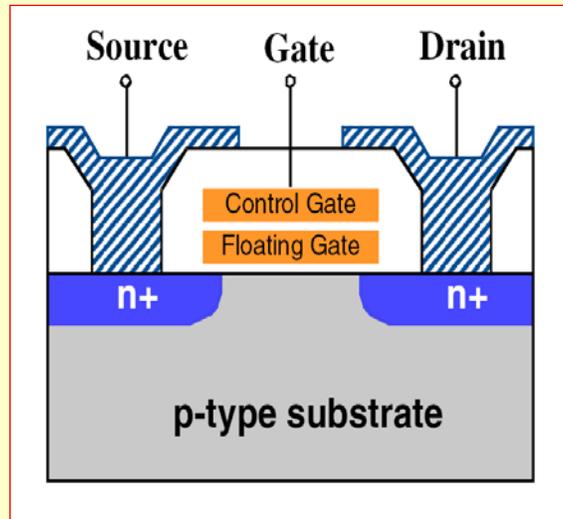
ROMs de máscara.  
PROMs



Memorias

14

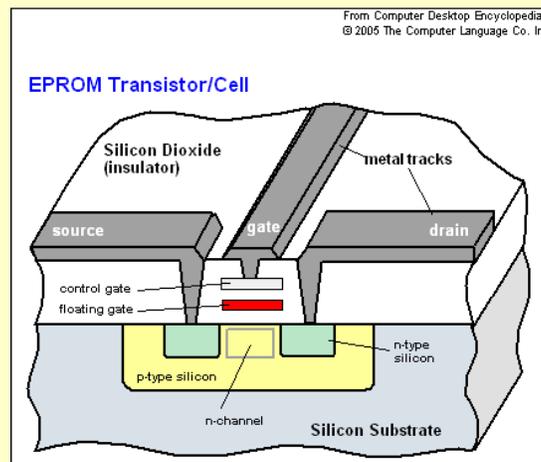
# Eproms



Memorias

15

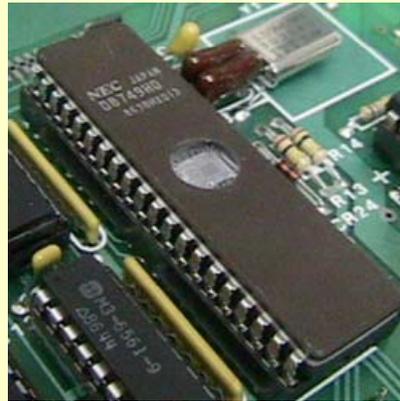
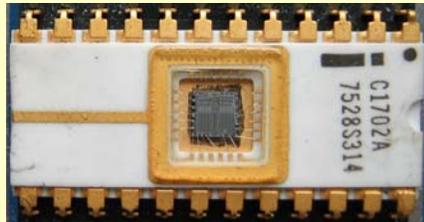
# Eproms



Memorias

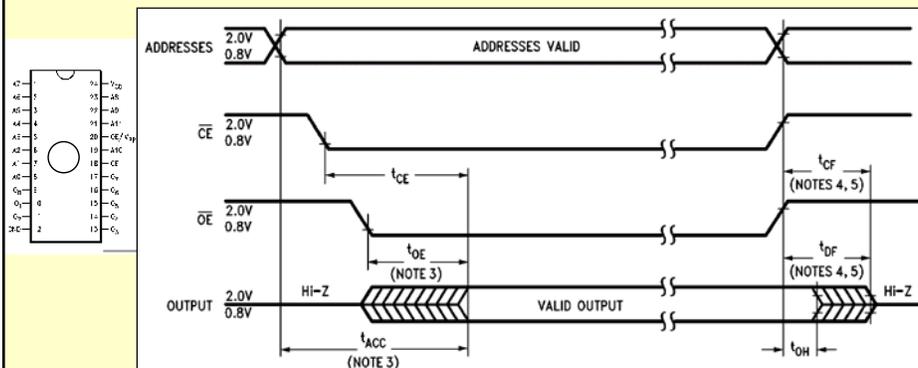
16

# EPROM



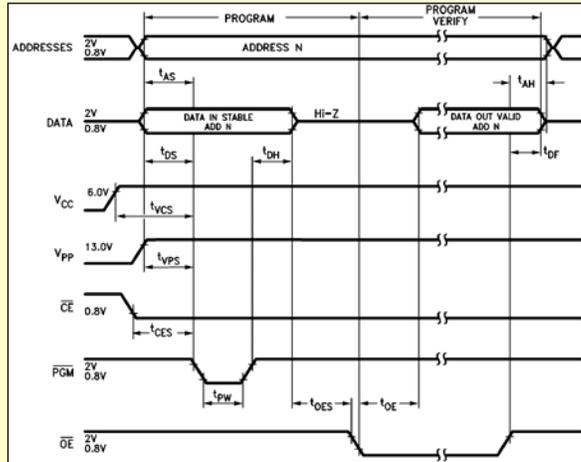
Memorias

# Eproms



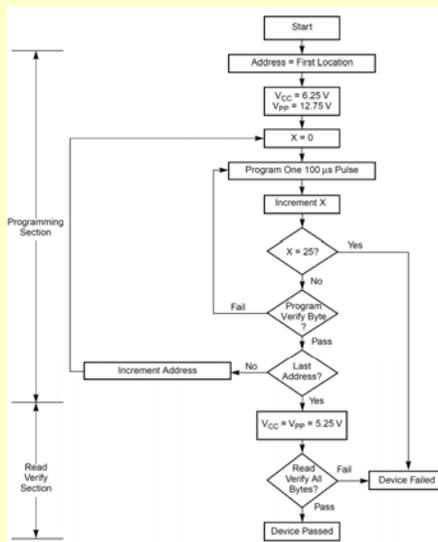
Memorias

# Programación EPROM



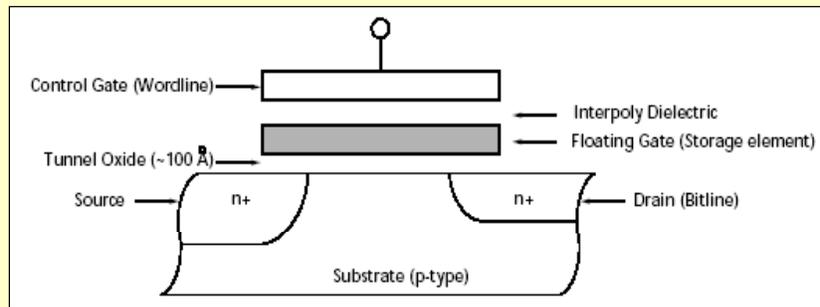
Memorias

# Programación Inteligente de EPROM



memorias

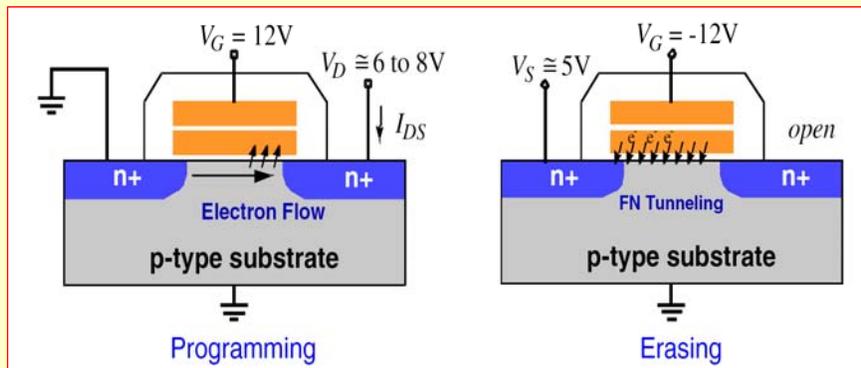
# Flash



Memorias

21

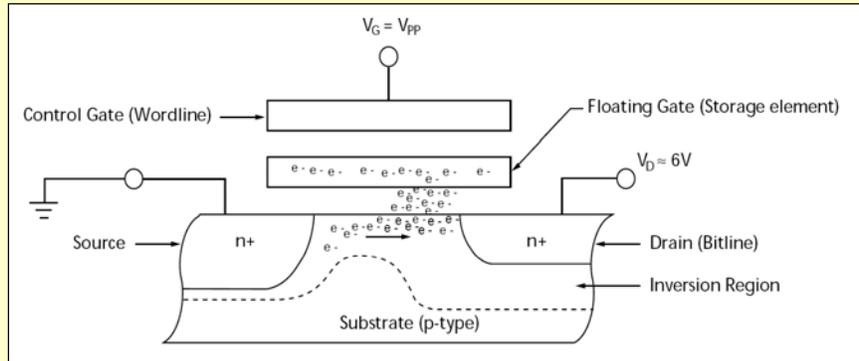
# Flash



Memorias

22

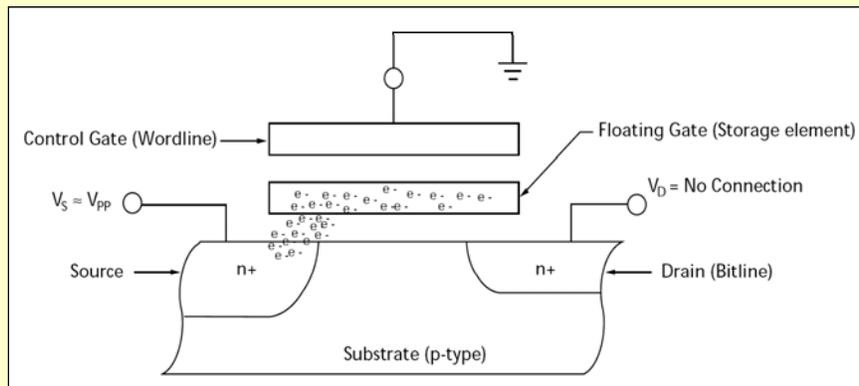
# Flash - Escritura



Memorias

23

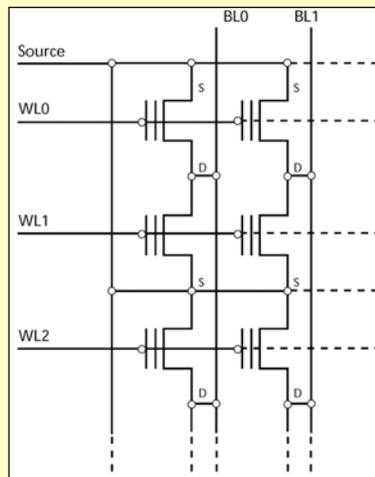
# Flash - Borrado



Memorias

24

# NOR Flash



Memorias

25

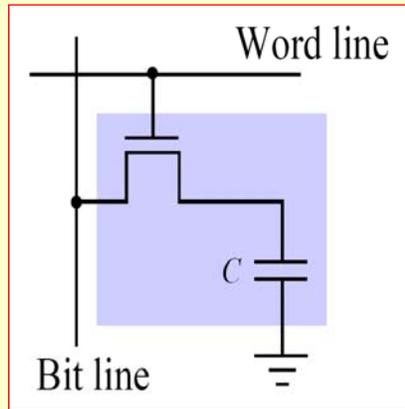
## Denominación de las Memorias

N	Significado
3	ROM
7	EPROM
8	E <sup>2</sup> PROM
9	FLASH

Memorias

26

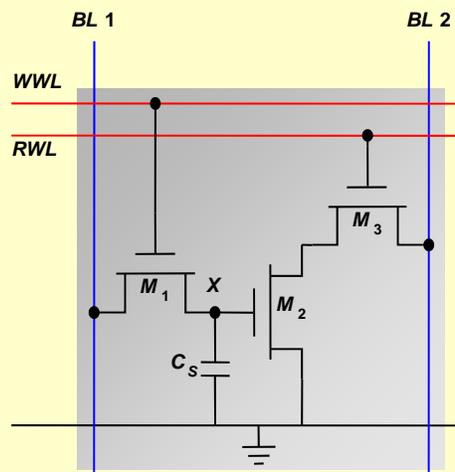
# Memorias Dinámicas



Memorias

27

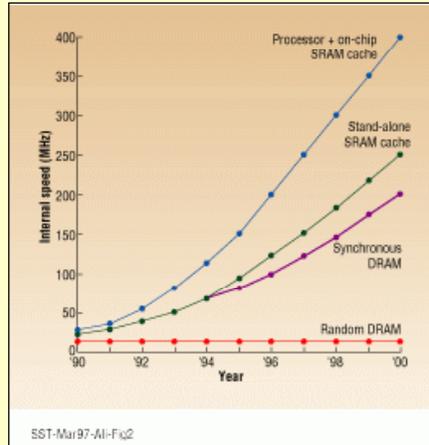
# Celda de 3 transistores



Memorias

28

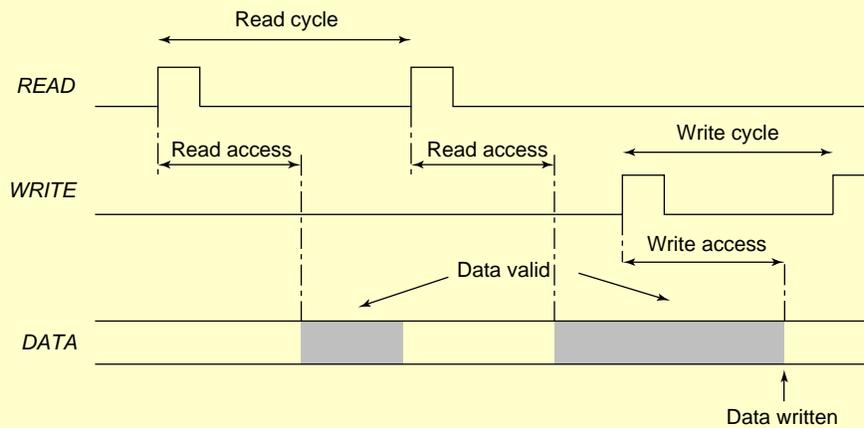
# Velocidades de Distintos Tipos



Memorias

29

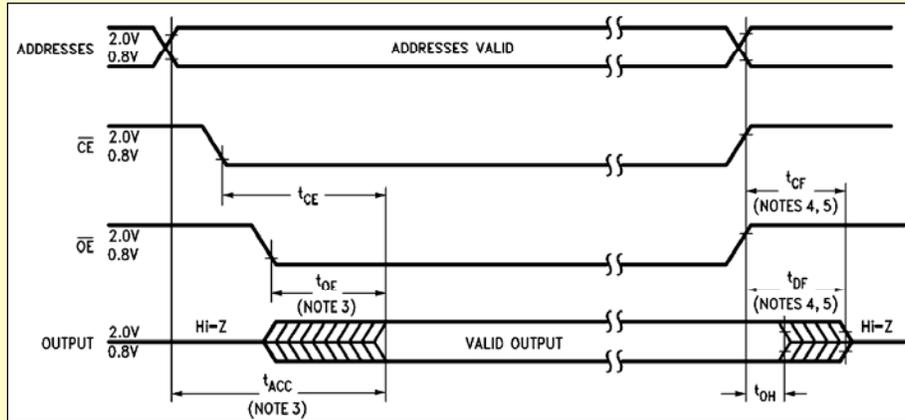
# Acceso



Memorias

30

## Tiempos de acceso



Memorias

31

## Tiempos de acceso

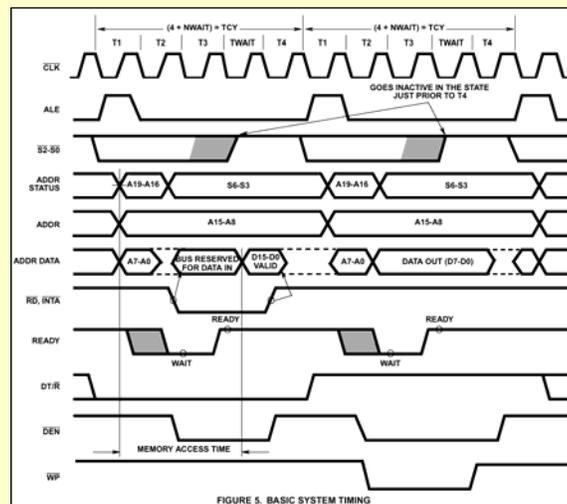
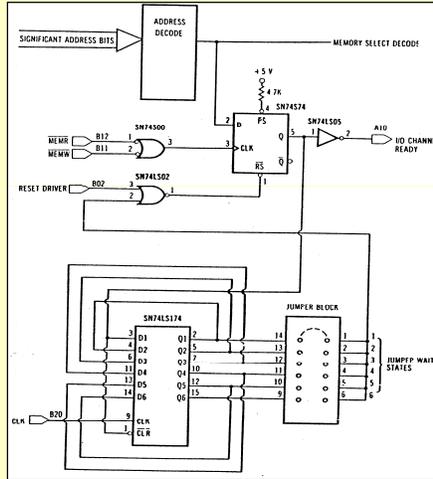


FIGURE 5. BASIC SYSTEM TIMING

32

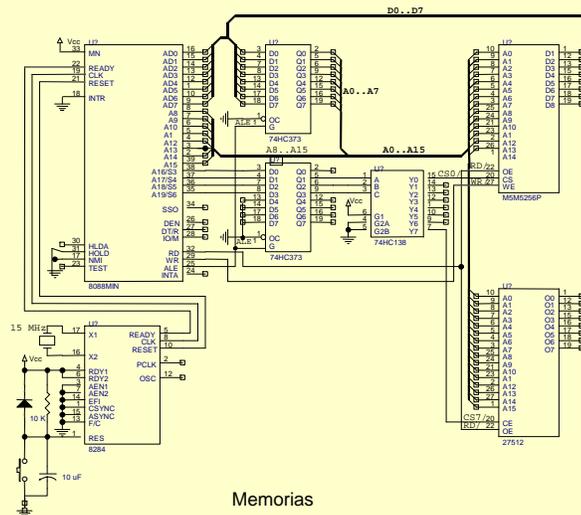
# Tiempos de Espera



Memorias

33

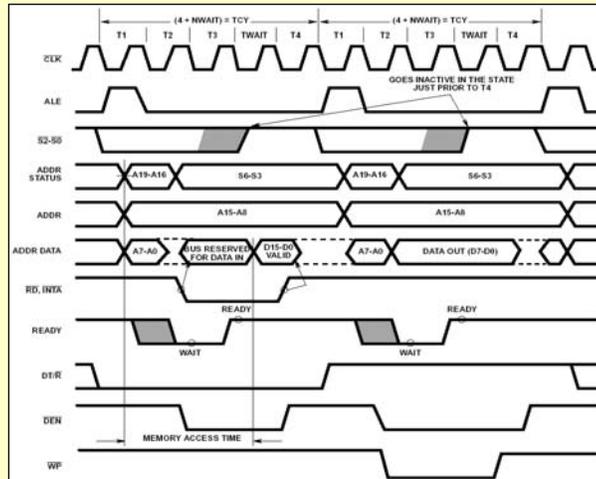
# Tiempo de Acceso



Memorias

34

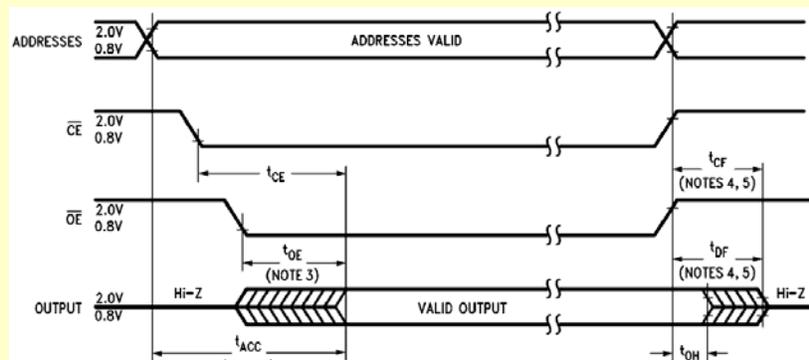
# Diagramas Temporales $\mu P$



Memorias

35

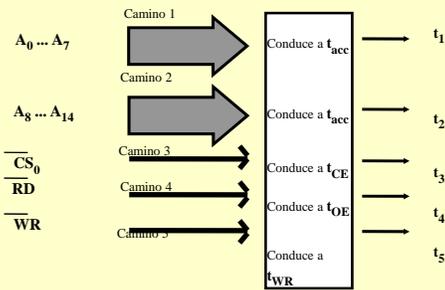
# Diagrama Temporal memoria



Memorias

36

# Tiempo de Acceso



Memorias

37

# Tiempo de Acceso

$$t_1 = t_{CLAV} + t_{p373} + t_{acc}$$

$$t_2 = t_{CLAV} + t_{acc}$$

$$t_3 = t_{CLAV} + t_{p373} + t_{p138} + t_{CE}$$

$$t_4 = t_{CLCL} + t_{CLRL} + t_{OE}$$

Memorias

38

# Tiempo de Acceso

Symbol	Parameters	Condition	Vcc	T <sub>A</sub> = 25°C		74HC	54HC	Units
				T <sub>A</sub> = -40° to 85°C		T <sub>A</sub> = -55° to 125°C		
				Typ	Guaranteed Limits			
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay, Data to Q	C <sub>L</sub> -50pF	2.0V	50	150	188	225	ns
		C <sub>L</sub> -150pF	2.0V	80	200	250	300	ns
		<b>C<sub>L</sub>-50pF</b>	<b>4.5V</b>	22	30	<b>37</b>	45	<b>ns</b>
		C <sub>L</sub> -150pF	4.5V	30	40	50	60	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay, Clock to Q	C <sub>L</sub> -50pF	6.0V	19	26	31	39	ns
		C <sub>L</sub> -150pF	6.0V	26	35	44	53	ns
		C <sub>L</sub> -50pF	2.0V	63	175	220	263	ns
		C <sub>L</sub> -150pF	2.0V	110	225	280	338	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay, Clock to Q	C <sub>L</sub> -50pF	4.5V	25	35	44	52	ns
		C <sub>L</sub> -150pF	4.5V	35	45	56	68	ns
		C <sub>L</sub> -50pF	6.0V	21	30	37	45	ns
		C <sub>L</sub> -150pF	6.0V	28	39	49	59	ns
	Maximum Output Enable Time	R <sub>L</sub> -1kΩ						

Memorias

39