FERNANDO LEONEL AGUIRRE

27 years, Electronic Engineer and Ph.D. Student

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orcid.org/0000-0001-7793-1194 researchgate.net/profile/FernandoAguirre7

WORK ENGAGEMENTS

R+D

UTN-FRBA, Laboratory of Nano-Electronics, Electronics Engineering Dept. / UIDI

April 2012 – present Bs. As., Argentina

- **PhD Student:** CMOS reliability on HK/high-mobility and mixed-signal IC Design (CONICET grant).

R+D

CNEA (Atomic Energy Commision of Argentina), Condensed Matter Group

April 2017 - May 2018 Bs. As. Argentina

- **PhD Student:** CMOS devices reliability and IC Design (CONICET grant).

Network administrator

UTN-FRBA, Electronics Engineering Dept.

April 2010 – March 2012 Bs. As., Argentina

- Network and servers administration (Linux) - Virtualization.

Support desk, Networking

Next Argentina

March 2009 - August 2009 Bs. As., Argentina

- Support desk for Linksys routers.

SKILLS

IC Design ●●●●●
- Familiar with Schematic, Layout and verification tools from Cadence, Mentor Calibre and Synopsys. Additional Knowledge of Verilog, SPICE, and printed circuit design

Electrical Characterization ●●●●●
- Extensive use of electrical characterization tools for semiconductor devices (C-V,I- T,I-V,etc.). Also knowledge in TCAD Sentaurus simulations.

Programming ●●●●●
- Experience coding in MATLAB, C, C++, BASH, Tcl, LaTeX, SPICE, Python and LabVIEW

Network administration ●●●●○
- Debian/RedHat(CentOs)-Linux based networks and Servers. Knowledge of Linux, MS Windows, and VMware virtualization.

MEMBERSHIPS

- IEEE (2010-present), IEEE-CAS (2016-present) and IEEE-EDS (2017-present)
- Electronics Engineering Dept. Council UTN-FRBA (2012-2016)
- Organizing committee of the 8th EAMTA / 7th CAMTA (2013) at UTN-FRBA
- Organizing committee of the 3rd ARGENCON (2016) at UTN-FRBA
- CASE 2017 Program Committee (2017)

TEACHING EXPERIENCE

Professor

UTN-FRBA

Abr 2018-present Bs. As., Argentina

- Analog IC Design (2018-present)

Teaching Assistant

UTN-FRBA

Abr 2013-present Bs. As., Argentina

- Applied Electronics I (2015-present)
- Analog IC Design (2013-present)

Invited Teaching Assistant

PUCRS

Oct. 2013 Porto Alegre, Brazil

- Introduction to analog IC design

LANGUAGES

Spanish ●●●●●
- Native speaker

English ●●●●●
- Highly proficient

German ●●●○○
- Professional working proficiency

EDUCATION

Graduate

UTN-FRBA

Mar 2017 – ongoing Bs. As., Argentina

- Ph.D. in Engineering | GPA: 7/10

Undergraduate

UTN-FRBA

Mar 2009–Dec 2016 Bs. As., Argentina

- Electronics Engineer | GPA: 7,97/10

Undergraduate stay in EE

Technische Universität Ilmenau

Sep 2014–Mar 2015 Thüringen, Germany

Secondary Education

Inst. Leonardo Murialdo

Mar 2006–Dec 2008 Bs. As., Argentina

- Electronic Technician | GPA 9,24/10

PUBLICATIONS

Main articles in refereed journals[1]

- **F. Palumbo, F. L. Aguirre, S. M. Pazos, I. Krylov, R. Winter, and M. Eizenberg (2018). "Influence of the spatial distribution of border traps in the capacitance frequency dispersion of Al2O3/InGaAs". In: *Solid-State Electronics***
- **F. Aguirre, S. Pazos, F. R. M. Palumbo, S. Fadida, R. Winter, and M. Eizenberg (2018). "Effect of forming gas annealing on the degradation properties of Ge-based MOS stacks". In: *Journal of Applied Physics* 123.13, p. 134103**
- **F. Palumbo, S. Pazos, F. Aguirre, R. Winter, I. Krylov, and M. Eizenberg (2017). "Temperature dependence of trapping effects in metal gates / Al_2O_3 / $InGaAs$ stacks". In: *Solid-State Electronics* 132, pp. 12–18**
- **S. M. Pazos, F. L. Aguirre, E. Miranda, S. Lombardo, and F. Palumbo (2017). "Comparative study of the breakdown transients of thin Al_2O_3 and HfO_2 films in MIM structures and their connection with the thermal properties of materials". In: *Journal of Applied Physics* 121.9, pp. 94–102**
- F. L. Aguirre, S. M. Pazos, G. M. Peretti, E. A. Romero, and S. Verrastro (2016). "Desempeño del método de análisis transitorio en la detección de fallas paramétricas en circuitos integrados". In: *UTN Proyecciones* 14.1
- F. L. Aguirre, O. Alpago, J. Atencio, A. Furfaro, S. M. Pazos, et al. (2015). "Diseño y síntesis de un Hasher SHA-256 en tecnología CMOS de 180nm". In: *UTN Proyecciones* 13.2, pp. 21–35
- S. M. Pazos, F. L. Aguirre, T. Mazur, G. Peretti, E. Romero, and S. Verrastro (2015). "Evaluación de la calidad de TRAM en la detección de fallas de fabricación en circuitos integrados analógicos fabricados en tecnología CMOS de 500nm". In: *UTN Proyecciones* 13.1, pp. 89–100

Main articles in refereed conference proceedings[1]

- **A. Fontana, S. M. Pazos, N. Vega, N. Müller, F. L. Aguirre, et al. "Heavy ion microbeam experimental study of ASET on a full-custom CMOS OpAmp". In: *SBCCI 2018***
- **A. Fontana, S. M. Pazos, F. L. Aguirre, N. Vega, N. Müller, et al. "Observation of heavy-ion induced ASET and charge sharing on a fullcustom CMOS OpAmp". In: *RADECS 2018***
- **S. M. Pazos, F. L. Aguirre, F. Silveira, and F. Palumbo (2018). "A Quality and Reliability Assessment Techniques and Methods for Devices and Systems". In: *ESREF 2018***
- **F. L. Aguirre, S. M. Pazos, F. Palumbo, S. Fadida, R. Winter, and M. Eizenberg (2018). "Impact of forming gas annealing on the degradation dynamics of Ge-based MOS stacks". In: *2018 IEEE International Reliability Physics Symposium (IRPS)*. IEEE, P–GD.3–1–P–GD.3–5**
- **F. L. Aguirre, S. M. Pazos, F. Palumbo, I. Krylov, and M. Eizenberg (2017). "Substrate influence on the behavior of capacitance hysteresis of III-V bilayered MOS stacks". In: *2017 32nd SBmicro*. IEEE, pp. 1–4**
- **S. M. Pazos, F. L. Aguirre, S. Lombardo, E. Miranda, and F. Palumbo (2017). "Experimental Study of Progressive Breakdown in Different Conductance States of Resistive Switching Structures". In: *China RRAM International Workshop 2017*. Soochow University, China**
- A. Fontana, S. M. Pazos, F. L. Aguirre, and F. Palumbo (2017). "Automatic ASET sensitivity evaluation of a custom-designed 180nm CMOS technology operational amplifier". In: *EAMTA 2017*. IEEE, pp. 21–25
- S. M. Pazos, F. L. Aguirre, and F. Palumbo (2017). "Charge trapping effects on Metal-Gate/High-k/III-V MOS devices assessed through C-V hysteresis". In: *EAMTA 2017*. IEEE, pp. 21–25
- S. M. Pazos, F. Palumbo, and F. L. Aguirre (2017). "Analysis and comparison of the CV-Dispersion of high-k, bi-layered MOS InGaAs/InP stacks". In: *PRIME-LA 2017*. IEEE, pp. 1–4
- F. L. Aguirre, S. M. Pazos, and F. Palumbo (2017). "Experimental study of progressive breakdown in different conductance states of resistive switching structures". In: *PRIME-LA 2017*. IEEE, pp. 1–4
- **F. Palumbo, S. M. Pazos, F. L. Aguirre, R. Winter, I. Krylov, and M. Einzenberg (2016). "Trapping and de-trapping effects of border traps in Metal Gates / Al2O3 / InGaAs stacks". In: *WoDiM 2016*. Catania, Italia**
- F. L. Aguirre, S. M. Pazos, G. M. Peretti, and E. A. Romero (2016). "A State-Variable Filter as a Case Study of the Transient Response Analysis Method". In: *ARGENCON 2016*. Buenos Aires, Argentina: IEEE, pp. 3–8
- S. M. Pazos, F. L. Aguirre, E. A. Romero, G. Peretti, and S. Verrastro (2015). "TRAM applied to second-order active filter designed in CMOS technology". In: *EAMTA 2015*. IEEE, pp. 47–52
- F. L. Aguirre, S. M. Pazos, J. Nowak, and D. Krausse (2015). "Procedimiento para el diseño de amplificadores de bajo ruido (LNA) utilizado en 806 y 1960 MHz". In: *Memorias del VI Congreso de Microelectrónica Aplicada*. La Matanza: Universidad de La Matanza, p. 6
- S. M. Pazos, F. L. Aguirre, and S. Verrastro (2015). "Técnicas de diseño contra fallas paramétricas y aplicación de un Amplificador Operacional CMOS". in: *Memorias del VI Congreso de Microelectrónica Aplicada*. Vol. 2. 3. La Matanza: Universidad de La Matanza

[1]Most relevant contributions are writen in black bold letters

HONORS AND DISTINCTIONS

Winner

- 3rd GPA E.E. 2017 UTN-FRBA (2018)
- Best published paper *PRIME - LA* (2017)
- CONICET Ph.D. grant (Argentina) (2016)
- EVC-CIN (University) grant (Argentina) (2015)
- UTN-DAAD grant (Germany) (2014)

Certifications

- Certificate in Advanced English (CAE) Grade B - University of Cambridge (2017)
- B2.1 (German Language) (2015)
- OnDaF test (German Language) B1 (2014)

Courses and Seminars

- Reliability and System Maintenance (2018)
- Estimation and Decision Theory (2017)
- Epistemology (2017)
- Design of analog Integrated Circuits (2017)
- Argentine School of Microelectronics (EAMTA)
  - Design and Test of Fault-Tolerant E.S. for Aerospace App. (2017)
  - Digital Track (2015)
  - Advanced topics in CMOS design (2014)
  - Analog track (2012)
- CMOS circuits (Germany)(2014)
- Techniques for design and testing of IC (2014)

Conferences and symposia

- IRPS 2018 (Burlingame, USA)
- SBmicro 2017 (fortaleza, BRA)
- LASCAS-PRIME 2017 (Bariloche, ARG)
- CAMTA:
  - 2017 (Bs. As., ARG)
  - 2015 (Villa María, ARG)
  - 2014 (Mendoza, ARG)
  - 2013 (Bs. As., ARG)
  - 2012 (Córdoba, ARG)
- SSCS Distinguished Lecturer Tour (IEEE) (2013)

REFERENCES

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Editor in chief, IEEE (Ret.)

Prof. Alejandro Furfaro
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Telecom (Ex.)